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# A COMPACT HIGH-GAIN SWITCHED-CAPACITOR CONVERTER FOR SUSTAINABLE ENERGY APPLICATIONS

JAYA CHRISTA SARGUNAR THOMAS[1], JAYANTHI KATHIRESAN[2], GNANAVADIVEL JOTHIMANI[3], MUTHU THIRUVENGADAM PERIYATHIRUVADI4

**Keywords: High-gain power converter; Green energy sources; Active switched-capacitor network; Electric Vehicles; On-board chargers; Low-voltage battery packs.**

**This research emphasizes the design and realization of a converter with enhanced voltage gain with the objective of ensuring efficient power extraction from low-voltage battery systems and diverse renewable energy sources. An active switched-capacitor network converter with a lower part count and continuous input current is introduced in this study. This designed converter accomplishes a maximum voltage gain of 30 at 0.8 duty cycle. The comprehensive theoretical analysis encompasses the converter's design, critical performance metrics, and a detailed efficiency assessment incorporating extensive loss calculations. A 100W hardware test bench for the designed converter showcases enhanced voltage gain with a stable 200 V on the higher potential side and a configurable 24V on the lower potential side. Moreover, the converter achieves a practical efficiency of 95% at rated load and exhibits robust performance under all tested source voltage and load-changing scenarios.**

## 1. INTRODUCTION

Electric Vehicles (EVs) are evolving as a new trend in the transportation sector. Mainly, the need for EVs has increased recently due to global concerns like the need for sustainable, green, and clean sources of energy, the impending energy crisis, as well as our reliance on traditional non-renewable energy sources. Implementing such modes of transportation requires knowledge of battery charging infrastructures, international charging guidelines, and upcoming developments in on-board chargers with efficient power conversion circuitry [1,2]. Literature [3] provides an in-depth overview of power processing converter configurations and battery pack design for energy storage, including its benefits, intricacies, and probable next-step advancements in EVs. In earlier days, converters with isolation capabilities were predominantly used to build up voltage levels to meet DC bus demands in EVs [4]. This isolated step-up converter adjusts the transformer's turns ratio to boost voltage levels. Besides, these converters with isolation impart certain drawbacks like voltage stresses on the secondary side, elevated ripples on input current, bulkier circuitry, and multiple power conversion stages. Figure 1 depicts the potential applications of DC–DC converter configurations with improved gain. Numerous studies [5,6] have explored several DC-DC structural layouts, including various modified versions of high-gain converters.

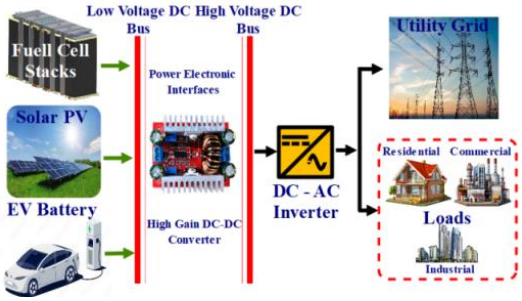



Fig. 1– Potential applications of elevated-gain DC–DC converter configurations.

Classical boost configurations are simple, but they incur elevated switch stress and static losses that result in poor conversion efficiencies at extremely high duty cycle operation. To overcome these limitations, cascaded boost and other step-up configurations have been reported in [7,8] to improve gain and operational range, but they compromise efficiency and power density and experience high device stresses. Also, a quadratic boost circuit and a buck-boost type power processing circuit with less ripple content [9,10] and an elevated-gain integrated quadratic boost topology with a dual switch applicable for EVs [11] are reported. Literature [12] provides a detailed review of several novel step-up (*i.e.*, high voltage conversion gain) topologies with improved efficiency, not with high duty ratios. Moreover, to lower the voltage across power switches, an idea of employing coupled inductors with a hybrid combination of two converters in the power circuitry to yield high voltage gain has gained prominence today [13,14]. However, increased electromagnetic interference noise, static and dynamic losses, and high voltage spikes over power switches are all caused by the connected inductor's leakage inductance. As another way to face these challenges, regenerative snubber circuitry or active clamped circuit designs are reviewed in [15], albeit doing so increases circuit intricacies and cost. Whereas, the non-coupled inductor circuits avoid such limitations and add certain benefits, viz., affordable cost, compact, lightweight, fewer circuit complications, and serve as a plausible solution for EV charging. Furthermore, many other boosting voltage structures like voltage lifters [16,17], multi-level boosters [18], active switched inductor (SL) networks [19], active switched capacitors (SCs) structure [20], SC network-coupled voltage multiplier [21], active switched LC configuration [22], extended gain (or) voltage lift schematics with SL [23,24], ultra-high gain topologies [25,26], and other high gain architectures [27,28] and their advanced control techniques are addressed in [29]. An idea of augmenting the voltage gain with multipliers and n-boosting stages suffers from a greater number of circuit elements and thereby increases complexity and cost. In this paper, an active network built with SCs is designed to achieve a considerable voltage conversion ratio, lower source current ripples, less switching stress on semiconductor elements, together with fewer circuit parts overall.

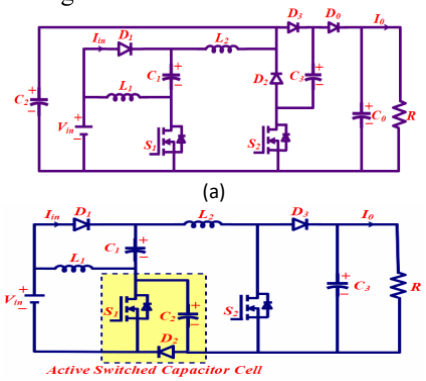
## 2. DESIGN AND DESCRIPTION OF THE PROPOSED CONVERTER

The proposed converter configuration is derived from the topology represented in Fig. 2(a). The representation of the

[1,2,3]Mepco Schlenk Engineering College, Sivakasi, Kariseri, Tamil Nadu 626005, India.
[4] AAA College of Engineering & Technology, Sivakasi, Tamil Nadu 626005, India.
E-mails: stchrista@mepcoeng.ac.in, kjayanthi@mepcoeng.ac.in, gvadivel@mepcoeng.ac.in, muthuthiruvengadam.p@aaacet.ac.in

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derived topology is depicted in Fig. 2(b), which has fewer components and increased voltage gain by adding an active switched capacitor cell across switch $S_1$. The converter is designed with dual power switches $S_1$ and $S_2$, switched capacitor cell $C_2$ and diode $D_2$, two inductors $L_1$ and $L_2$, diodes $D_1$ & $D_3$, boosting capacitor $C_1$, and filter capacitor $C_3$. The following assumptions are considered while designing the converter: (i) the inductors $L_1$ and $L_2$ are ideal; (ii) the parasitic resistances are neglected; (iii) loads can be supported by an adequate size of output capacitor. The converter proposed in Fig. 2(b) operates in two states based on its switching characteristics.



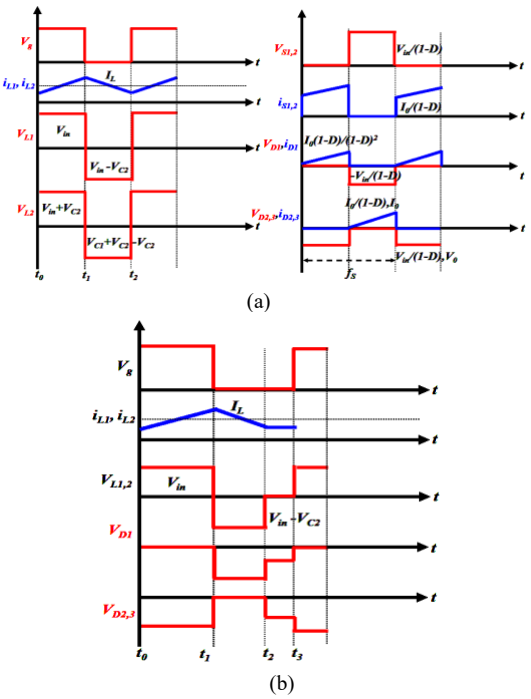

(a)

(b)

Fig. 2 – (a) Converter topology in [35]; (b) Configuration of the derived converter.

## 3. STATIC GAIN EXPRESSION FOR PROPOSED CONVERTER AT CCM

The switching waveforms for continuous and discontinuous conduction mode (CCM, DCM) are represented in Fig. 3(a,b).



(a)

(b)

Fig. 3 – Switching waveforms: (a) CCM; (b) DCM.

### 3.1 OPERATING STATE 1 ($T_0$ - $T_1$)

In operating state 1, the power MOSFETs $S_1$ and $S_2$ are activated, whereas the diodes $D_2$ and $D_3$ are in the blocked state, and diode $D_1$ is in a forward-bias condition. Figure 4(a) indicates the current flow path for State 1.

$$V_{in} = V_{L1} = V_{C1}, V_{L2} = V_{C2} + V_{in},$$

$$V_{C3} = V_0, I_{C1} = I_{in} - I_{L1} - I_{L2}, I_{C2} = I_{L2}, I_{C3} = -I_0. \quad (1)$$

### 3.2 OPERATING STATE 2 ($T_1$ – $T_2$):

During operating state 2, power MOSFETs $S_1$ and $S_2$ are inactivated, and power diodes $D_3$ and $D_2$ are in the conducting state, and $D_1$ is in the non-conducting state. Figure 4(b) indicates the current flow path throughout the time $(1\text{-}D)Ts$,

$$V_{L1} = V_{in} = V_{C1}, V_{L2} = V_{in} + V_{C2}, V_{C3} = V_0,$$
$$I_{C1} = I_{in} - I_{L1} - I_{L2}, I_{C2} = I_{L2}, I_{C3} = -I_0. \quad (2)$$

Using the volt-sec balancing concept for the inductors, voltage $V_{C2}$ is expressed as

$$V_{C2} = \frac{V_{in}}{(1-D)}, \quad (3)$$

and the voltage conversion ratio as,

$$\frac{V_0}{V_{in}} = \frac{(2-D)}{(1-D)^2}. \quad (4)$$

## 4. STATIC GAIN EXPRESSION FOR THE PROPOSED CONVERTER AT DCM

The converter's analysis in DCM is supported by its switching waveform as shown in Fig. 3(b).

1) *Operating State 1* ($T_0$ - $T_1$)

This functional state corresponds to operating state 1 in CCM. Power MOSFETs are activated, and the schematic is pictured in Fig. 4(a). The inductor voltages are computed as

$$V_{L1} = V_{in}, V_{L2} = V_{in} + V_{C2}, V_{C3} = V_0. \quad (5)$$

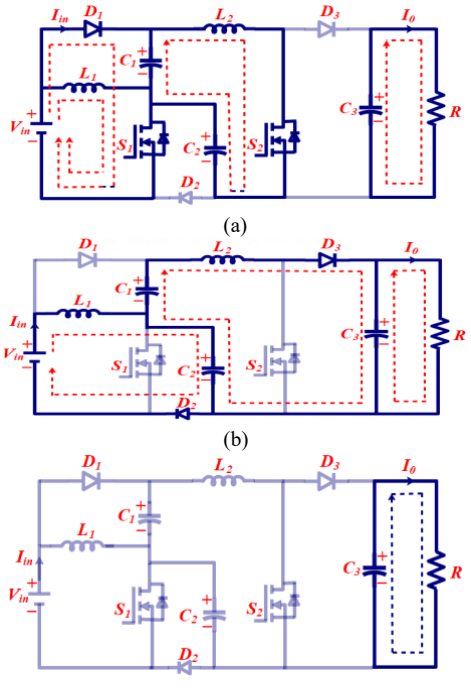
2) *Operating State* 2 ($T_1$ – $T_2$)

Two power MOSFETs are inactivated in this interval. The current tracing during this period is shown in Fig. 4(b). The inductor current decreases throughout this time interval. The voltage expressions are computed as in eq. (6)

$$V_{L1} = V_{in} - V_{C2}, V_{L2} = V_{C2} + V_{in} - V_0, V_{C3} = V_0. \quad (6)$$

3) *Operating State* 3 ($T_2$ – $T_3$)

Two power MOSFETs are inactivated, and inductor currents are zero during this state. The output capacitor powers the load. The current path for this interval is shown in Fig. 4(c).



(a)

(b)

(c)

Fig. 4 – Operational states of the designed configuration with its current paths: (a) State 1; (b) State 2; (c) State 3.

The expression for the output is

$$V_{C3} = V_0. \quad (7)$$

The expression is demonstrated by employing the volt-second balancing concept over inductor $L_1$.

$$\int_0^{D_1T} V_{L1}\mathrm{d}t + \int_0^{D_2T} V_{L1}\mathrm{d}t + \int_0^{(1-D_1-D_2)T} V_{L1}\mathrm{d}t = 0. \quad (8)$$

On substituting the VL1expressions in states 1, 2, and 3, the capacitor voltage $V_{C2}$ is given as

$$V_{C2} = \frac{V_{in}(D_1 + D_2)}{D_2}. \quad (9)$$

Similarly, on applying the volt-second principle to inductor $L_2$, the voltage conversion ratio in DCM is obtained,

$$\int_0^{D_1T} V_{L2}\mathrm{d}t + \int_0^{D_2T} V_{L2}\mathrm{d}t + \int_0^{(1-D_1-D_2)T} V_{L2}\mathrm{d}t = 0, \quad (10)$$

$$\frac{V_0}{V_{in}} = \frac{D_1D_2 + {D_2}^2 + (D_1 + D_2)^2}{{D_2}^2}. \quad (11)$$

## 5. DESIGN CONSIDERATIONS

1) *Design equations of $L_1$ and $L_2$*

For the modeled converter to be in CCM, the values of inductances $L_1$ and $L_2$ are selected according to the switching frequency, duty cycle ($D$), ripple currents, and input voltage ($V_{in}$). Expressions (1, 2) are utilized to design $L_1$ and $L_2$ values. To manipulate the inductance values,

$$L_1 \geq \frac{V_{in}\,DT}{\Delta \mathrm{I_{L1}}};\ L_2 \geq \frac{V_{in}D^2}{\Delta \mathrm{I_{L2}}(1-D)f}. \quad (12)$$

2) *Selection of $C_1$ and $C_2$*

The values of capacitors $C_1$, $C_2$, and $C_3$ rely on output current, the capacitor's ripple voltage, duty ratio, and switching frequency,

$$C_1 \geq \frac{(2-D)\mathrm{I_0}D}{(1-D)^2 2\Delta \mathrm{V_{C1}f}};\ C_2 \geq \frac{(2-D)\mathrm{I_0}D}{(1-D)^2 2\Delta \mathrm{V_{C2}f}};$$

$$C_3 \geq \frac{\mathrm{I_0}D}{\Delta \mathrm{V_{C3}f}}. \quad (13)$$

3) *$I_{L1}$ and $I_{L2}$ Expressions*

By applying the current-sec balancing principle to capacitor currents $I_{C2}$ and $I_{C3}$, the expressions for the inductive currents are computed as shown in

$$I_{L1} = \frac{I_0(1+2D)}{(1-D)^2};\ I_{L2} = \frac{I_0}{1-D}. \quad (14)$$

4) *$I_{C2}$ and $I_{C3}$ Expressions*

The capacitor current expressions are obtained by substituting and simplifying the inductor current expressions and are expressed as:

$$I_{C1} = \frac{I_0(1+D)}{(1-D)^2};\ I_{C2} = \frac{I_0D}{1-D};$$

$$I_{C3} = \frac{I_0D}{I_0D}. \quad (15)$$

5) *Selection of Switches $S_1$ and $S_2$*

The power switch selection depends on the current through the switch while it is conducting and the voltage across the switch while it is not conducting. Voltage and current values are computed based on the equations below.

6) *$V_{S1}$ and $V_{S2}$ Voltages*

The switches $S_1$ and $S_2$ are inactivated during the second operating state. $V_{S1}$ voltage during this period is equal to $V_{C2}$ voltage. $V_{S2}$ is the same as the output voltage and is mentioned in:

$$\mathrm{V_{S1}} = V_{C2} = \frac{V_{in}}{1-\mathrm{D}};\ \mathrm{V_{S2}} = \mathrm{V_0}. \quad (16)$$

7) *$I_{S1}$ and $I_{S2}$ Currents*

Like the switch voltages, the currents $I_{S1}$ and $I_{S2}$ are computed during state 1 operation. The $I_{S1}$ current is equivalent to the input current $I_{in,}$ and the $I_{S2}$ current is equivalent to $I_{L2}$ or $I_{C2}$ and is given by

$$I_{S1} = I_{in} = \frac{(2-D)I_0}{(1-D)^2};\ I_{S2} = I_{L2} = I_{C2} = \frac{I_0}{1-D}. \quad (17)$$

8) *Selection of $D_1$, $D_2$, and $D_3$*

Voltage and current during the operating states are considered to select $D_1$, $D_2$, and $D_3$.

9) *$V_{D1}$, $V_{D2}$ and $V_{D3}$ Voltages*

The voltage across the diodes is calculated based on their operating states. The diode $D_1$ is in ON state during the period $0 < t < DT_s$ whereas $D_2$ and $D_3$ are in ON state during $DT_s < t < T_s$ period. Voltage stress is computed in the inactive state of the diodes. The voltage expressions are:

$$V_{D1} = \frac{-V_{in}}{1-D};\ \mathrm{V_{D2}} = V_{C2} = \frac{V_{in}}{1-D};\ V_{D3} = V_{C3} = V_0. \quad (18)$$

10) *$I_{D1}$, $I_{D2}$ and $I_{D3}$ Currents*

Similarly, the currents through the diodes are calculated and are represented as follows.

$$I_{D1} = I_{in} - I_{L1} = \frac{I_0(1+D)}{(1-D)^2}, \quad (19)$$

where, $I_{L1}$ is the inductor $L_1$ current, $I_0$ is output current

$$I_{D2} = I_{C2} + I_{C3} + I_0. \quad (20)$$

On substituting $I_{C2}$ and $I_{C3}$ values, the simplified $I_{D2}$ expression is given as

$$I_{D2} = \frac{I_0(1+D)}{1-D}, \quad (21)$$

$$I_{D3} = I_{L2} = \frac{I_0}{1-D}, \quad (22)$$

where $I_{L2}$ is the current in Inductor $L_2$.

## 6. ELECTRICAL POWER LOSS STUDY

In the realm of power converters, the internal resistance of all the circuit components plays a crucial role in determining their efficiency. This is because the parasitic resistances of these elements significantly contribute to power loss. So, it is imperative to consider the consequences of these parasitic elements on the effectiveness of the converter and overall efficiency.

*Table 1*

Power loss estimation in various devices.

| S. No. | Devices in the Power Circuit | RMS and Average Currents | Power Loss Estimated |
|---|---|---|---|
| 1 | $D_1$, $D_2$, $D_3$ | $I_{D1rms} = \frac{I_0(1+D)\sqrt{D}}{(1-D)^2}$=3.41A<br>$I_{D1}^{avg} = \frac{I_0(1+D)D}{(1-D)^2}$ = 2.598 A | $P_D^{Loss} = V_f I_{D1}^{avg}$<br>$+r_{D1}I_{D1rms}^2 + V_f I_{D2}^{avg}$ +<br>$+r_{D2}I_{D2rms}^2 + V_f I_{D3}^{avg}$<br>$+r_{D3}I_{D3rms}^2$= 2.89 W |
| 2 | $C_1$, $C_2$, $C_3$ | $I_{C1rms} = \frac{I_0(1+D^2)}{\sqrt{1-d}}$ =1.59A<br>$I_{C2rms} = \frac{I_0D}{\sqrt{1-d}}$=0.69A<br>$I_{C3rms} = \frac{V_0D}{R_L\sqrt{(1-D)}}$= 0.69A | $P_C^{Loss} = I_{C1rms}^2 r_{C1}$ +<br>$+I_{C2rms}^2 r_{C2} + r_{C3}I_{C3rms}^2$=<br>=0.28 W |
| 3 | $L_1$ and $L_2$ | $I_{L1rms} = \frac{V_0(1-2D)}{R(1-D)^2}$=0.45A<br>$I_{L2rms} = \frac{V_0}{R(1-D)}$= 1.19 A | $P_L^{Loss} = I_{L1rms}^2 r_{L1}$ +<br>$+r_{L2}I_{L2rms}^2$ = 0.162 W |
| 4 | $S_1$ and $S_2$ | $I_{S1_rms} = I_{in}\sqrt{D}$= 3.16 A<br>$I_{S2_rms} = \frac{I_0\sqrt{D}}{(1-D)}$= 0.91 A | $P_S^{Loss}$ =<br>$= \frac{I_{S1_{ON}}V_{S_{off}}(T_{ON}+T_{OFF})f_s}{2}$ +<br>$+I_{S_rms}^2 r_{DS}$= 2.13 W. |

This section deals with the impact of parasitic resistance on

power loss. The following equivalent series resistance values are taken into consideration for estimating the power loss: $r_{L1} = r_{L2} = 0.01\ \Omega$, $r_{d1} = r_{d2} = r_{d3} = 0.1\ \Omega$, $r_{c1} = r_{c2} = 0.08\ \Omega$, $r_{c3} = 0.13\ \Omega$, $r_{DS} = 0.1\Omega$, $T_{ON} = 23$ ns, $T_{off} = 150$ ns, $V_f = 0.8$ V.

Ultimately, using the following expressions, the total power losses and efficiency for the designed topology have been computed.

$$P_{Loss} = P_L^{Loss} + P_C^{Loss} + P_D^{Loss} + P_S^{Loss};$$
$$Efficiency = \frac{P_0}{P_0 + P_{Loss}}. \quad (23)$$

After substituting the loss values in the above equation, the total power loss is about $P_{Loss} = 5.49$ W. Figure 5 depicts the distribution of power losses within the designed converter. It is inferred that inductor power loss is less than that of capacitors, diodes, and switches. The derived converter efficiency is about 95% under rated conditions, while experimental efficiencies of this new topology at various load conditions are shown in Fig. 6.

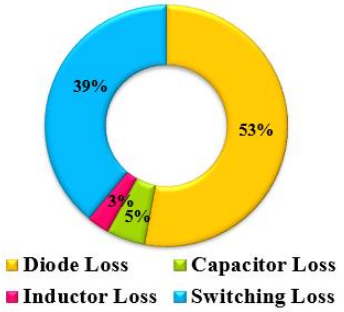



Fig. 5 – Breakdown of power loss in individual components.

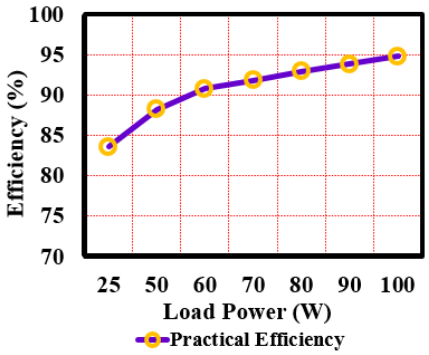



Fig. 6 – Efficiency *Vs* load power.

## 7. COMPARATIVE ANALYSIS

Table 2 lists the detailed comparison study of the designed converter structure with other similar configurations.

*Table 2*

Comparative study of converters.

| Ref. | L | C | S | D | TCC | Voltage Gain | Voltage Stress across Switches | Voltage across Diodes | Efficiency (%) |
|---|---|---|---|---|---|---|---|---|---|
| Boost Conv. | 1 | 1 | 1 | 1 | 4 | $\frac{1}{(1-D)}$ | $V_0$ | $V_0$ | - |
| 5 | 3 | 3 | 2 | 2 | 10 | $\frac{1+3D}{1-D}$ | $\frac{V_{in}}{1-D}$ | $\frac{2V_{in}}{1-D}$ | 93% |
| 17 | 3 | 4 | 2 | 3 | 12 | $\frac{2(1+D)}{1-D}$ | $\frac{V_0}{2(1-D)}$ | - | 93.1% |
| 18 | 2 | 6 | 2 | 6 | 16 | $\frac{3+D}{1-D}$ | $\frac{V_{in}}{1-D}$ | $\frac{V_{in}}{1-D}$ | - |
| 19 | 4 | 3 | 2 | 5 | 14 | $\frac{3+D}{1-D}$ | $\frac{2V_{in}}{1-D}$ | $\frac{V_{in}}{1-D}$ | 93.6 |
| 27 | 2 | 4 | 2 | 4 | 12 | $\frac{4}{(1-D)}$ | $\frac{V_0}{4}, \frac{V_0}{2}$ | $\frac{V_0}{4}, \frac{V_0}{2}$ | 96.5% |
| Proposed conv. | 2 | 3 | 2 | 3 | 10 | $\frac{(2-D)}{(1-D)^2}$ | $\frac{V_{in}}{1-D}$, $V_0$ | $\frac{V_{in}}{1-D}$, $V_0$ | 95% |

The comparisons are made with respect to total component count (TCC), voltage across switches and diodes. The proposed structure exhibits a maximal gain of 30, whereas the converters in [27,19,5,18,17] have static gains of 20,19,17,18 respectively, and the corresponding plot is shown in Fig. 7. Likewise, the TCC of the proposed structure is 40% less when compared with [18], and the comparison plot is shown in Fig. 8. It also depicts the total count of inductive elements (NL), capacitive elements (NC), power switches (NS), and power diodes (ND) used in the different configurations.

Switching voltage stress is almost 50% less in the proposed converter when compared with [19], and the corresponding voltage stress plot is depicted in Fig. 9.

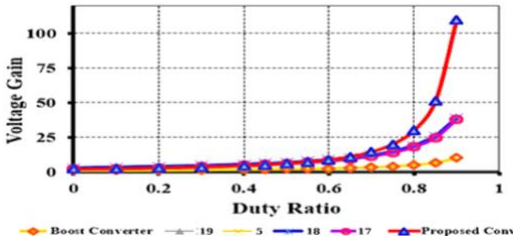



Fig. 7 – Voltage gain as a function of duty ratio profile.

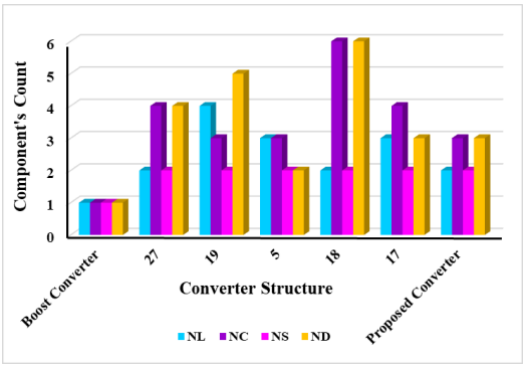



Fig. 8 – Component count comparison across different converter structures.

*Table 3*

Hardware Particulars of the converter

| Parameters | Values |
|---|---|
| Input Voltage ($V_{in}$) | 24 V |
| Inductors $L_1$&$L_2$ | 1 mH, 1.4 mH |
| Switching Frequency | 20 kHz |
| Capacitors $C_1$and $C_2$ | 100 µF |
| Load Power | 100 W |
| Output capacitor $C_3$ | 220 µF |
| Diode | STTH30R04 |
| MOSFET | IRF520 |
| Output Voltage ($V_o$) | 200 V |

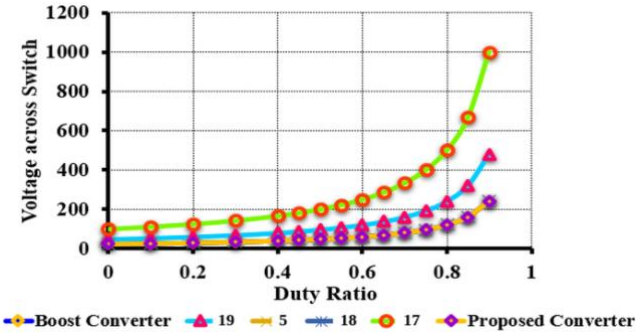



Fig. 9 – Plot of switch voltage stress versus duty ratio.

## 8. SIMULATION AND HARDWARE RESULTS

To verify the theoretical ideas, the designed topology is simulated in MATLAB/Simulink. Figure 10 depicts the closed-loop simulation waveforms of the proposed topology for a resistive load. A regulated voltage output of 200 V is

obtained at an output current of 0.5 A when 24 V is given as input. The converter behavior is found to be the same for an inductive load too.

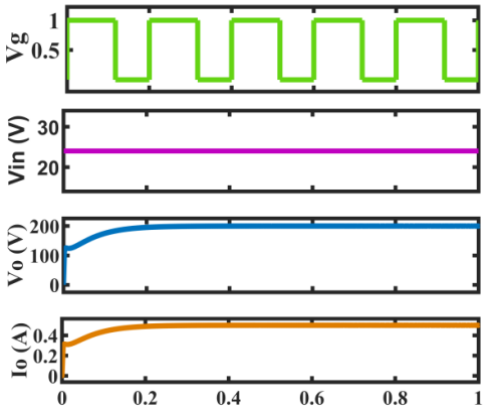
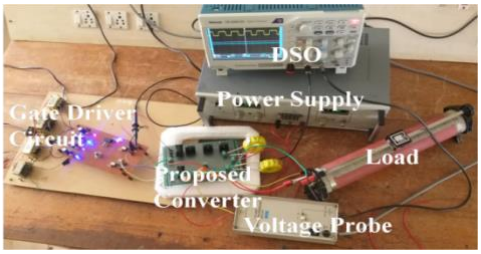
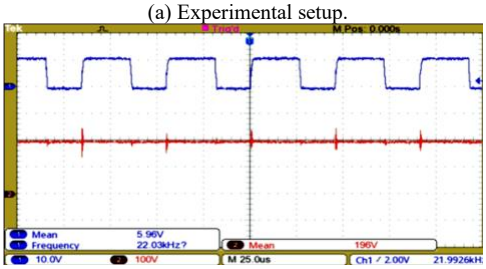



Fig. 10 − Simulation waveforms of gating pulse, supply voltage, output voltage, and output current.

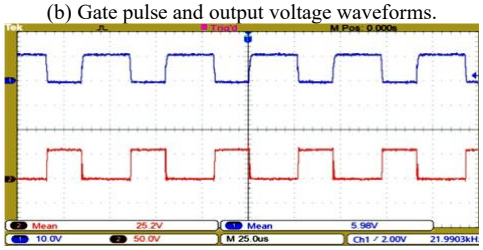
A 100 W laboratory test bench setup of the proposed topology is constructed for validating the simulation findings. Circuit specifications are tabulated in Table 3. Figure 11 depicts the hardware prototype, waveforms of output voltage, switch voltages, and diode voltages, which give a clear picture of the converter's functionality. The proportional-integral controller maintains an output voltage of 200 V. Figure 11(h,i) shows the inductor current waveforms.



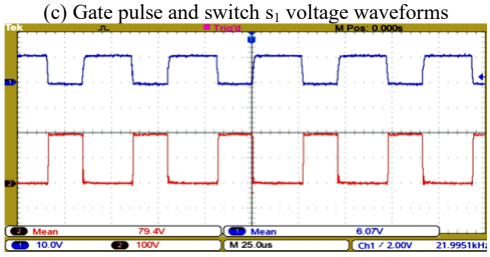

(a) Experimental setup.



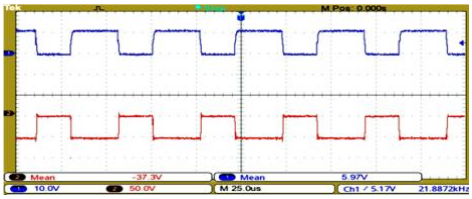
(b) Gate pulse and output voltage waveforms.



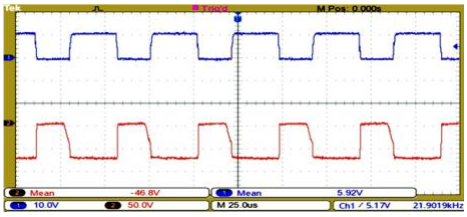
(c) Gate pulse and switch $s_1$ voltage waveforms



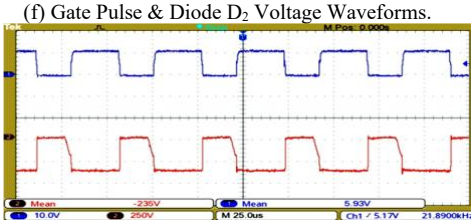
(d) Gate pulse and switch $S_2$ voltage waveforms



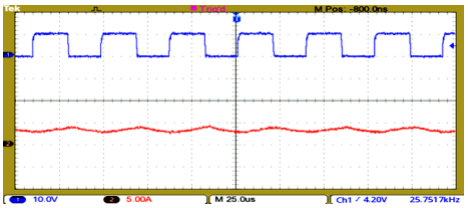
(e) Gate pulse and diode $D_1$ voltage waveforms



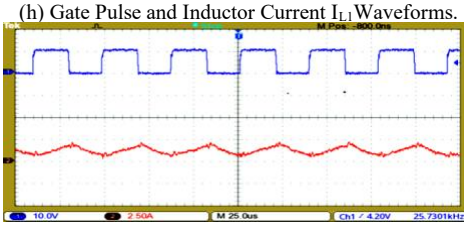
(f) Gate Pulse & Diode $D_2$ Voltage Waveforms.



(g) Gate pulse and diode $D_3$ voltage waveforms.



(h) Gate Pulse and Inductor Current $I_{L1}$ Waveforms.



(i) Gate pulse and inductor current $I_{L2}$ waveforms

Fig. 11 – The hardware prototype, waveforms of output voltage, switch voltages, and diode voltages

The dynamic fluctuations in load power and source voltage are demonstrated in Fig. 12. The functionality of the modeled converter is validated by varying the supply voltage from 20 V to 24 V, and the resulting changes in output voltage are illustrated in Fig. 12(a). Likewise, the transient behavior for load power variation is pictured in Fig. 12(b). The controller continuously monitors variations in the voltage, determines the corresponding error signal, and delivers the control signal to obtain the regulated voltage output. The settling time to reach the steady-state value of the voltage output is around 40 ns, as shown in Fig. 12. These waveforms ensure that the output voltage is controlled precisely, evidencing a reliable and efficient performance of the designed structure.

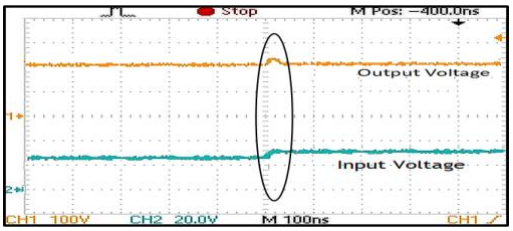



Fig. 12 – (a) Source voltage variation waveforms. Vertical axis: output voltage (100V/div), input voltage (20 V/div). Horizontal axis: Time (100 ns/div).

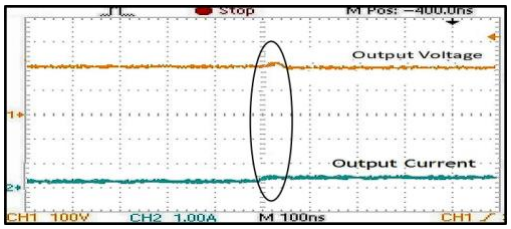



Fig. 12 – (b) Load power variation waveforms. Vertical axis: voltage (100 V/div), current (1 A/div). Horizontal axis: time (100 ns/div).

## 9. CONCLUSION

A novel switched capacitor-based active network converter has been constructed for sustainable energy applications. The step-up converter lessens the stresses on the diodes as well as the switches, and the $L^2C^2D^2$ arrangement, together with the active switched-capacitor network, boosts the output voltage with high voltage conversion gain in single-stage power conversion. The avoidance of magnetic coupling greatly lowers the circuit's size and cost, which provides additional merits to this converter. The hardware outcomes of the converter show enhanced voltage gain and efficiency. Finally, an in-depth comparative analysis is made on the performance of the suggested converter amongst other converters on par, as stated in the literature.

## CREDIT AUTHORSHIP CONTRIBUTION STATEMENT

Jaya Christa Sargunar THOMAS: Conceptualization, manuscript preparation.
Jayanthi KATHIRESAN: Converter design.
Gnanavadivel JOTHIMANI: Experimental validation.
Muthu Thiruvengadam PERIYATHIRUVADI: Mathematical analysis.

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