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A NOVEL MODULAR REDUCED COMPONENT MULTISOURCE MULTILEVEL INVERTER FOR SUSTAINABLE APPLICATIONS

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Keywords: Multisource; Modular; Renewable; Reduced components; Total harmonic distortion.

This paper introduces a novel modular multi-source multilevel inverter (MSMLI) topology tailored for renewable energy applications. The proposed architecture features a compact basic unit comprising nine switches, three DC voltage sources, and an H-bridge polarity-reversal circuit. With equal source magnitudes, this module produces a 7-level output; configuring the sources in a 1:3 ratio extends the output to 15 levels. By connecting multiple units in series, higher voltage levels can be achieved efficiently in both symmetric and asymmetric modes. Crucially, only four switches need to be active per level, minimizing switching losses and improving overall efficiency. Total harmonic distortion (THD) is significantly reduced—from 12.20% in symmetric operation to 5.38% in asymmetric mode—enhancing waveform quality. Generalized mathematical expressions support both level-generation control strategies. Comparative evaluation with existing inverter topologies demonstrates advantages in switch count, THD, and total standing voltage (TSV). The theoretical analysis was validated by experimental results obtained from a laboratory-built prototype. The multi-source capability and low hardware complexity make this MSMLI ideal for integration with sustainable applications.

1. INTRODUCTION

As the pursuit of cleaner and more efficient energy grows, solar and wind power are increasingly taking a leading role in modern electricity production. As these systems become more widespread, the demand for reliable, flexible, and cost-effective power conversion technologies has increased significantly. Among the various power electronic converters, multilevel inverters have attracted considerable attention for their ability to generate clean voltage waveforms while keeping harmonic content and electromagnetic interference to a minimum. [1]. Their ability to synthesize near-sinusoidal output waveforms with reduced harmonic content, lower voltage stress, and improved efficiency makes them well-suited for solar, wind, and hybrid systems. Traditional multilevel inverter topologies such as diode-clamped, flying capacitor, and cascaded H-bridge (CHB) configurations have proven effective in many applications. However, they often require a large number of switches, bulky passive components, or isolated DC sources, making them less suitable for compact and cost-sensitive renewable energy systems. These challenges have driven ongoing research into topologies that can achieve a higher number of output levels with fewer switches and sources, without compromising efficiency or waveform quality. [2,3] proposed an asymmetric MLI with less number of switches. Their design demonstrated effective THD suppression and was particularly suitable for generating higher voltage levels. However, their topology still relied on isolated DC sources and lacked scalability, making it less suitable for modular or distributed applications. In another approach, [4] developed a modified CHB-based topology tailored for hybrid systems incorporating solar and wind sources. While their inverter design achieved lower THD and employed fewer switches than conventional CHB structures, it still involved ten MOSFETs and additional control circuitry. Moreover, their work was validated through simulations only, with no hardware implementation reported. A combination of half-bridge units and an H-bridge to produce a 15-level inverter output is explored in [5]. This design utilized 21 switches and isolated DC inputs to enhance waveform quality. Though their simulation results were promising, the requirement for multiple isolated sources and the relatively high switch count could pose challenges in real-world deployment, especially in cost-sensitive environments. A more recent contribution by [6] introduced a reduced-switch asymmetric inverter that generated up to 15 levels using only eight switches and four DC sources. Their work emphasized control, simplicity, and reduced switching effort. However, the topology's voltage configuration became increasingly complex as more levels were added, limiting its scalability. A different perspective was offered by [7], who developed a single-source, nine-level inverter using a minimal number of switches and a PWM-based control strategy. The design achieved effective THD suppression and lower hardware complexity. However, its single-source limitation makes it unsuitable for multi-source systems such as those found in solar–wind hybrid networks. [8-12] proposes the switched-capacitor-based multilevel inverters. The capacity to increase the output voltage, increase output levels, and reduce components are some of the characteristics of switched capacitors [12]. Capacitors in multilevel inverters that are charged and discharged at high frequencies undergo damage and have lower lifespans and may experience early failure due to increased stress from sporadic voltage spikes, improper loads, or insufficient switching [13]. From the above studies, it is evident that while many designs aim to reduce component count and improve harmonic performance, they often do so at the expense of scalability, source flexibility, or experimental validation. These limitations motivated the present work, which focuses on developing a modular, multi-source multilevel inverter with minimum switches. The proposed inverter uses a simple basic unit consisting of nine switches and three DC sources, enhanced by an H-bridge for polarity inversion. This topology supports both symmetric and asymmetric configurations and requires only four switches to be active at a time. Importantly, the design has been validated not only through simulations but also with a hardware prototype, making it a practical solution for renewable energy integration. The salient features of the proposed design are

- Supports both symmetric and asymmetric operation
- Modular and easily scalable design
- Low total harmonic distortion (THD)
- Polarity inversion using H-bridge
- Only four switches conduct per voltage level
- No use of diodes or capacitors

The rest of the paper is arranged in the following sequence: Section 2 introduces the developed inverter

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topology along with its switching configurations. Section 3 outlines the pulse-width modulation strategy employed in the design. The logic gate-based control implementation is presented in Section 4. Section 5 explores how the topology can be extended for higher voltage levels or additional modules. Section 6 discusses the key results and their practical significance, while Section 7 concludes the work with final remarks and future considerations.

2. DEVELOPED MSMLI TOPOLOGY

The newly developed MSMLI design is depicted in the Fig. 1 below.

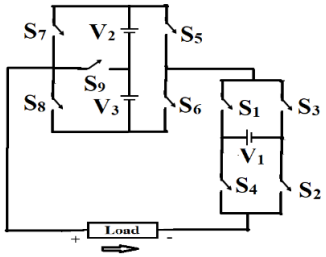

Fig. 1 – Proposed MSMLI topology

The basic module of the topology consists of 2 DC sources and 5 switches, and it is connected to the H-bridge via 4 switches and 1 DC source. This circuit generates 7 levels when all the voltage magnitudes are equal and produces 15 levels with the ratio of 1:3. The switching pattern for the symmetric mode is shown in Table 1.

Table 1

Switching Sequence – 7 level.

Switches/ Levels	1	2	3	4	5	6	7	8	9
1	☑	☑	☒	☒	☑	☒	☑	☒	☒
2	☑	☑	☒	☒	☒	☑	☒	☒	☑
3	☑	☑	☒	☒	☒	☑	☑	☒	☒
-1	☒	☒	☑	☑	☑	☒	☑	☒	☒
-2	☒	☒	☑	☑	☑	☒	☒	☒	☑
-3	☒	☒	☑	☑	☑	☒	☒	☑	☒
0	☒	☑	☑	☒	☑	☒	☑	☒	☒

Table 2

Switching Sequence – 15 level.

Switches/ Levels	1	2	3	4	5	6	7	8	9
1	☑	☑	☒	☒	☑	☒	☑	☒	☒
2	☒	☒	☑	☑	☒	☑	☒	☒	☑
3	☑	☒	☒	☑	☒	☑	☒	☒	☑
4	☑	☑	☒	☒	☒	☑	☒	☒	☑
5	☒	☒	☑	☑	☒	☑	☑	☒	☒
6	☑	☒	☒	☑	☒	☑	☑	☒	☒
7	☑	☑	☒	☒	☒	☑	☑	☒	☒
-1	☒	☒	☑	☑	☑	☒	☑	☒	☒
-2	☑	☑	☒	☒	☑	☒	☒	☒	☑
-3	☒	☑	☑	☒	☑	☒	☒	☒	☑
-4	☒	☒	☑	☑	☑	☒	☒	☒	☑
-5	☑	☑	☒	☒	☑	☒	☒	☑	☒
-6	☒	☑	☑	☒	☑	☒	☒	☑	☒
-7	☒	☒	☑	☑	☑	☒	☒	☑	☒
0	☒	☑	☑	☒	☑	☒	☑	☒	☒

The switching sequence during the asymmetric mode of operation is shown in Table 2. The voltage magnitude is taken in the ratio of 1:3. To generate any level of output, only four switches conduct at a time. irrespective of the operating modes of the topology. By following the switching sequence as mentioned in Tables 1 and 2, the required number of levels can be generated.

The power flow diagram for randomly selected output levels is illustrated in Fig. 2.

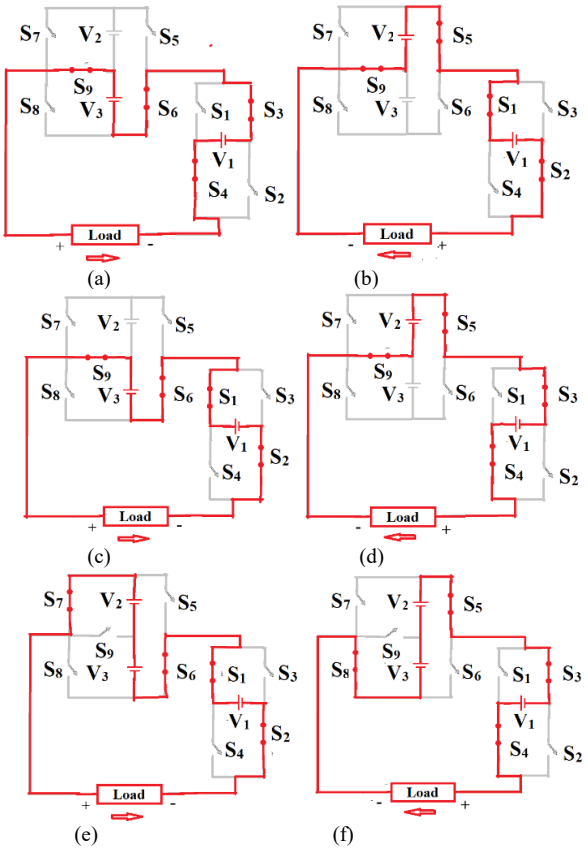

Fig. 2 – Power flow diagram of voltage levels a) $2V_{dc}$ b) $-2V_{dc}$ c) $4V_{dc}$ d) $-4V_{dc}$ e) $7V_{dc}$ f) $-7V_{dc}$.

The switches S_1-S_4 are useful for obtaining positive and negative polarity outputs. The voltage source V_1 is fixed as V_{dc} for both the symmetric and asymmetric modes of operation.

3. MULTICARRIER PULSE WIDTH MODULATION

Multicarrier pulse width modulation (MC-PWM) has become a popular control strategy in multilevel inverter applications, particularly due to its simplicity, flexibility, and ability to generate high-quality output waveforms. Unlike traditional PWM methods used in two-level inverters, MC-PWM involves the comparison of a single reference signal (usually a sine wave) with multiple carrier signals to establish the conducting states of the power devices. In multilevel inverter systems, the number of carrier signals depends on the number of output voltage levels desired. For an *m*-level inverter, $(m-1)$ carrier signals are required. These carriers are typically arranged either in a parallel or staggered configuration, and several carrier-based schemes can be implemented, such as:

- Phase disposition (PD): All carriers are in-phase and aligned vertically.
- Phase opposition disposition (POD): Carriers above and below the zero reference are phase-shifted by 180°.
- Alternative phase opposition disposition (APOD): Each carrier is alternately phase-shifted by 180° relative to the adjacent one.

Among these, phase disposition (PD) is often preferred for its lower total harmonic distortion (THD) in line-to-line voltage outputs. In this method, all triangular carrier signals are in phase, which simplifies implementation and helps minimize

total harmonic distortion (THD) in the output waveform — a key objective in this work. The integration of MC-PWM with the proposed MSMLI topology ensures precise voltage control, efficient switch utilization, and high-quality output suitable for renewable energy systems where waveform purity and reliability are essential.

It is important to note that the number of carrier signals is determined by the required number of output voltage levels rather than the number of power semiconductor devices. In the proposed topology, separate carrier sets are employed for the positive and negative half cycles to achieve voltage level generation. The use of seven carriers per half cycle (P_1 to P_7) and (N_1 to N_7.) enables accurate synthesis of the intended multilevel output with proper level sequencing and reduced harmonic distortion. Employing a smaller number of carriers, such as four, would limit the achievable voltage levels and compromise the output waveform quality.

The sinusoidal reference signal has a frequency of 50 Hz (f_m) and an amplitude of 7 V. Each triangular carrier wave operates at a frequency of 1 kHz (f_c) with an amplitude of 1 V. Gating signals are generated by comparing the sinusoidal reference signal with the corresponding carrier signals. These gate pulses are then applied to the switches following the predefined switching logic, enabling the inverter to synthesize the required output voltage levels.

4. LOGIC GATE IMPLEMENTATION

In this topology, fourteen gating signals are generated, corresponding to the number of carrier waves employed. However, with only nine power switches available, applying each gate pulse directly to a switch is impractical. This mismatch makes direct implementation of gating signals challenging, especially in simulation, where logic-based control must be manually defined. To overcome this, a logic gate-based control circuit was developed specifically for the simulation environment. Logical expressions, derived from the inverter's switching pattern, were used to generate the necessary gate signals for each switch. These expressions, presented in eq. (1) to (9), dictate the switching logic and were implemented using basic digital logic components such as AND, OR, and NOT gates.

$$S_1 = (P_1 \oplus P_2 \oplus P_3 \oplus P_5 \oplus P_6) + (N_2 \oplus N_3 \oplus N_5 \oplus N_6) \quad (1)$$
$$S_2 = (P_1 \oplus P_2 \oplus P_4 \oplus P_5 \oplus P_7) + (N_2 \oplus N_4 \oplus N_5 \oplus N_7) \quad (2)$$
$$S_3 = \overline{(P_2 \oplus P_3 \oplus P_5 \oplus P_6)} \oplus \overline{(N_1 \oplus N_2 \oplus N_3 \oplus N_5 \oplus N_6)} \quad (3)$$
$$S_4 = \overline{(P_2 \oplus P_4 \oplus P_5 \oplus P_7)} \oplus \overline{(N_1 \oplus N_2 \oplus N_4 \oplus N_5 \oplus N_7)} \quad (4)$$
$$S_5 = \overline{P_1 \oplus P_2 \oplus N_1} \quad (5)$$
$$S_6 = P_2 \quad (6)$$
$$S_7 = (P_1 \oplus P_2 \oplus P_5) + (N_1 \oplus N_2) \quad (7)$$
$$S_8 = \overline{N_5} \quad (8)$$
$$S_9 = (P_2 \oplus P_5) + (N_2 \oplus N_5) \quad (9)$$

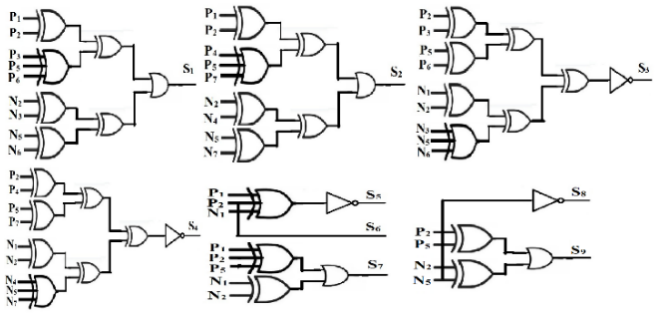

Fig. 3 – Logic Gate Implementation

Figure 3 illustrates how these logic gates were configured to synthesize accurate gating pulses within the simulation framework.

5. MODULAR VERSION OF PROPOSED TOPOLOGY

One notable strength of the suggested inverter design is its modular structure, which allows for straightforward scalability. The basic unit—comprising nine switches, three DC sources, and an H-bridge for polarity inversion—can be replicated and connected in series to form an extended version of the topology, capable of generating a higher number of output voltage levels. The extended topology is shown in the Fig. 4 below.

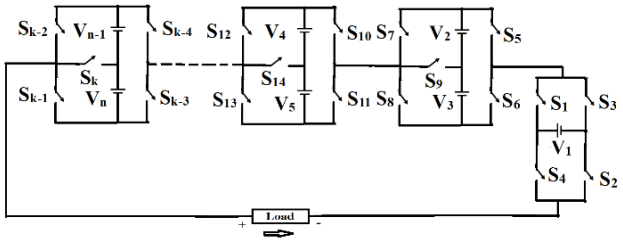

Fig. 4 – Extended Topology

In the extended configuration, each additional module contributes new intermediate voltage steps, increasing the resolution of the output waveform. This results in smoother transitions between voltage levels, lower harmonic distortion, and improved power quality. Whether operating in symmetric or asymmetric mode, the output voltage can be precisely shaped by selecting appropriate values for the DC sources within each module. For every module added, the number of switches is increased by 5, and the number of DC voltage sources is increased by 1. Furthermore, the control strategy scales with the topology. Each module follows the same switching logic, and the overall control system can be expanded using either centralized or distributed architectures. In simulation, additional logic expressions are derived based on the extended switching pattern to accommodate the increased number of levels. Let us consider $N_{BM\ to}$ be the number of basic modules, $N_{DC\ to}$ be the number of sources, N_{level} to be the number of levels, and $N_{k\ to}$ be the number of switches. The generalized equations to determine the number of levels, number of switches, and DC sources for N_{BM} modules connected in series are derived below for both symmetric and asymmetric operation, as shown in Table 3 below.

Table 3

Generalized equations for the extended topology.

Algorithm	N_{DC}	N_k	N_{level}
Symmetrical	$2N_{BM}+1$	$5N_{BM}+4$	$4N_{BM}+3$
Asymmetrical	$2N_{BM}+1$	$5N_{BM}+4$	$3\ X\ 5^{N_{BM}}$

The above table shows that the number of DC sources and the number of switching devices needed remain the same irrespective of operating modes. But the number of levels increases drastically in the asymmetrical mode just by changing the voltage ratio. This makes the proposed topology more effective with fewer components.

6. COMPARISON OF PROPOSED TOPOLOGY WITH CONVENTIONAL TOPOLOGIES

The comparison table 4 presents a detailed analysis of various multilevel inverter (MLI) topologies reported in the literature and the proposed configurations. The topologies are evaluated based on five essential hardware parameters: the number of DC sources (N_{DC}), power switches (N_k), clamping components such as capacitors (N_c) and diodes (N_d), and the achievable output voltage levels (N_{level}).

Topologies such as those in [14], [16], and [17] require a relatively larger number of DC sources to achieve the desired output levels. For instance, the configuration in [17] uses an equal number of DC sources and switches, which increases the hardware burden as the number of output levels increases. Overall, the comparison highlights that the proposed topology offers a more efficient and compact design, outperforming many existing solutions in terms of component count and performance trade-offs. On the other hand, designs like [15,19,22] use fewer DC sources—often just one—by increasing the number of switches and gate drivers, leading to more complex switching structures. Some configurations, such as [18,20], scale rapidly with respect to the number of switching devices as output levels increase.

In contrast, the proposed symmetric topology generates multiple output levels using a balanced configuration of switches and sources.

Table 4

Comparison with other topologies.

Paper / Parameters	N_{DC}	N_k	N_C	N_d
[14]	$\frac{N_{level}-1}{2}$	$N_{level}+1$	Nil	$\frac{N_{level}-1}{2}$
[15]	1	$N_{level}+1$	$\frac{N_{level}-2}{2}$	$\frac{N_{level}-2}{2}$
[16]	$\frac{N_{level}-1}{2}$	$\frac{N_{level}+5}{2}$	Nil	Nil
[17]	$\frac{N_{level}-9}{6}$	$\frac{N_{level}-9}{2}$	Nil	Nil
[18]	$\frac{N_{level}-1}{2}$	$\frac{4N_{level}-4}{3}$	Nil	Nil
[19]	$\frac{N_{level}-1}{4}$	$N_{level}-1$	$\frac{N_{level}-1}{4}$	$N_{level}-1$
[20]	$\frac{N_{level}-1}{8}$	$\frac{11(N_{evell}-1)}{8}$	$\frac{N_{level}-1}{4}$	$\frac{N_{level}-1}{8}$
[21]	$\frac{N_{level}-1}{8}$	$N_{level}+1$	$\frac{N_{level}-1}{4}$	$\frac{N_{level}-1}{8}$
[22]	$\frac{N_{level}-1}{2}$	$N_{level}-1$	Nil	Nil
Proposed Symm	$\frac{N_{level}-1}{2}$	$\frac{5N_{level}+1}{4}$	Nil	Nil
Proposed Asymm	$2\log_5\frac{N_{level}}{3}+4$	$5\log_5\frac{N_{level}}{3}+4$	Nil	Nil

No additional clamping components like capacitors or diodes are required. The proposed asymmetric topology is optimized for hardware efficiency. It reduces the number of DC sources and switches using a logarithmic relation. This design achieves high-resolution output voltage with a significantly lower hardware count. Clamping elements are not used, and the number of gate drivers equals the number of switches. Overall, both proposed topologies demonstrate better scalability and reduced hardware complexity compared to many existing designs, especially in minimizing DC sources and eliminating clamping components while maintaining the ability to produce a high number of output voltage levels.

7. RESULTS AND DISCUSSIONS

To validate its operation, the proposed inverter topology was simulated in MATLAB/Simulink. For this analysis, each DC voltage source was set to 100 V. The gating signals required for the nine switches were generated using a level-shifted pulse width modulation (PWM) strategy. To assess the inverter's output characteristics, the output voltage, output current, and the harmonic profile—obtained via Fast Fourier Transform (FFT) analysis—were examined under a purely resistive load of 90 Ω. These simulation results are illustrated in Fig. 5.

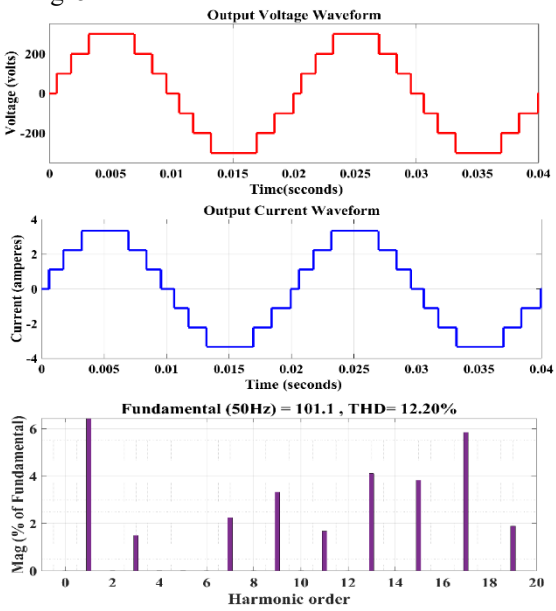

Fig. 5 – Simulation results of Symmetrical 7-level inverter - Output voltage, Output current, and FFT analysis for R=90 Ω

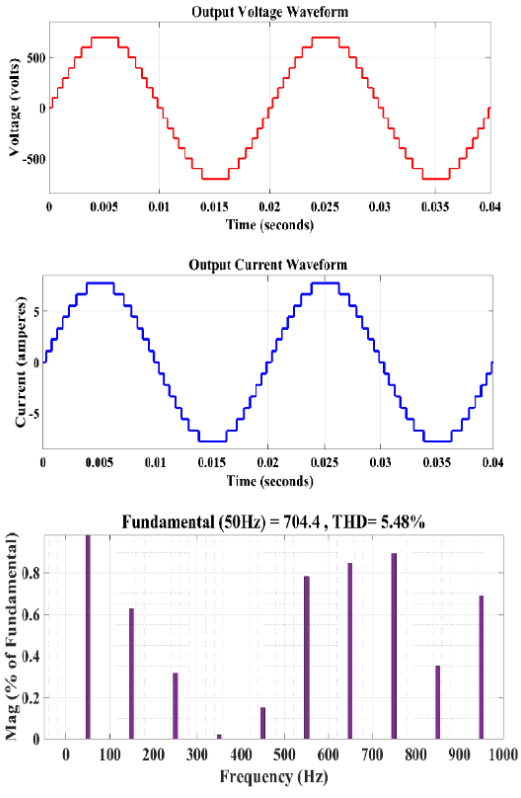

Fig. 6 – Simulation results of Asymmetrical 15 level inverter - Output voltage, Output current, and FFT analysis for R=90 Ω

The total harmonic distortion is 12.20 % for the seven-level

output produced. To further reduce the harmonics, the same topology is operated in asymmetric mode with V1 = 100 V and $V_2 = V_3 = 300$ V. The resistive load of 90 Ω is considered for the asymmetrical mode too. The output waveforms of the asymmetric mode are shown below in Fig. 6. The total harmonic distortion is reduced to 5.48% under the asymmetric mode of operation. Just by changing the magnitude of the voltage source to the ratio of 1:3, the quality of the output voltage is increased. A carrier switching frequency of 1 kHz is used to operate the converter. Nevertheless, the output voltage's perceived or effective switching frequency is larger than the carrier frequency because of the multilevel PWM technique. The FFT spectrum of the 15-level output voltage shows that the initial dominating switching harmonics are pushed towards higher frequency bands instead of arriving at 1 kHz, and the fundamental component appears at 50 Hz. As a result, output voltage quality is enhanced, and low-order harmonics are decreased.

The simulation results for RL load under various power factors for 7-level and 15-level were also obtained and shown in Table 5 below, respectively. Table 5 presents the variation of voltage THD, current THD, and power factor for different combinations of resistive and inductive loads. The resistance was fixed at 90 Ω, while the inductance was gradually decreased from 2051 mH to 0 mH to observe its impact on harmonic performance.

Table 5

Load analysis of a 7-level and a 15-level multilevel inverter.

Load Parameters		Power factor	7 Level		15 Level	
Resistance (Ω)	Inductance (mH)		Voltage THD (%)	Current THD (%)	Voltage THD (%)	Current THD (%)
-	2051	0	12.20	39.84	5.48	38.93
90	1432	0.2	12.20	35.84	5.48	34.88
90	656	0.4	12.20	31.69	5.48	30.67
90	381	0.6	12.20	22	5.48	25.84
90	214.8	0.8	12.20	25.42	5.48	19.21
90	-	1	12.20	12.20	5.48	5.48

From the data, it is evident that the voltage THD remains constant across all test cases, regardless of the load configuration. This confirms that the harmonic content of the output voltage is primarily influenced by the inverter's switching strategy and modulation technique, not by the nature of the load. In contrast, the current THD shows a clear dependence on the inductance of the load. Higher inductance values result in increased current distortion. As the inductance decreases, current THD gradually drops, reaching a minimum for the purely resistive case. The power factor improves as inductance is reduced, progressing from 0 (pure inductive) to 1 (pure resistive). This aligns with the expectation that inductive loads introduce a lagging power factor due to phase shifts between voltage and current, while resistive loads maintain a unity power factor. These results highlight the critical role of load parameters in shaping the harmonic behaviour of inverter-fed systems. While voltage harmonics are invariant, the current waveform becomes progressively cleaner as the system transitions from inductive to resistive loading. This insight is particularly important when designing inverters for applications with variable load characteristics, such as motor drives or renewable energy systems with dynamic operating conditions. The hardware implementation for a 7-level output is shown in Fig. 7.

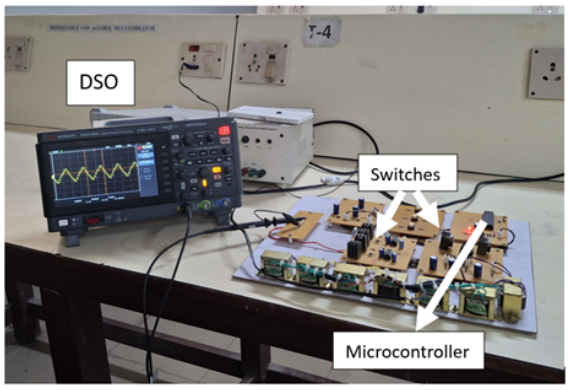

Fig. 7 – Hardware implementation.

The proposed topology is verified using the laboratory prototype. The IRF840 MOSFET switches are used, and the DSPIC30F4011 microcontroller is used to generate the gating pulses. The TLP250 gate driver circuit is employed with a resistive load of 130 MΩ. The DC sources are realized using transformers and a voltage regulation circuit. The maximum blocking voltage across any power semiconductor device is restricted to 2 Vdc, or 16 V in the current design, according to the voltage stress analysis of the proposed converter. Therefore, in this work, commercially available IRF840 MOSFETs rated for a drain-source voltage of 500 V are used. This guarantees dependable and useful execution of the suggested topology and offers a sizable safety margin. The output voltage waveform for a 7-level inverter is shown in Fig. 8.

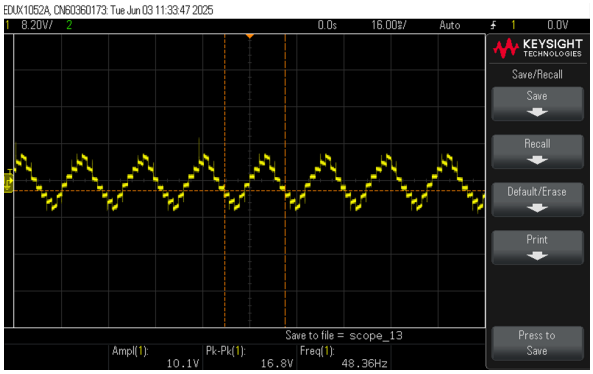

Fig. 8 – Output voltage waveform.

8. CONCLUSION

This research introduces a novel multisource modular multilevel inverter (MSMLI) topology that utilizes only nine switches and three DC voltage sources. Designed to function efficiently in both symmetric and asymmetric modes, the topology incorporates a polarity-reversing H-bridge to reduce hardware complexity while delivering high-quality output. In symmetric mode, the inverter generates a 7-level output using equal DC sources. In asymmetric mode, a non-uniform voltage ratio of 1:3 enables the same configuration to produce 15 output levels without adding extra components, highlighting the system's scalability and flexibility. Gating signals were developed using level-shifted PWM, with logical expressions implemented for simulation, and a microcontroller was used to generate optimized hardware pulses. MATLAB/Simulink simulations validated the performance, showing significantly reduced total harmonic distortion (THD), particularly in the asymmetric mode. Harmonic analysis confirmed that voltage THD remained

nearly constant across varying load conditions, while current THD was strongly influenced by the load's inductance. A noticeable improvement in power factor was observed with decreasing inductance, confirming the inverter's robust performance under practical loading. With a compact design, reduced switch count, and minimal passive components, the proposed MSMLI offers a highly efficient and modular solution for applications involving asymmetrical or independent DC sources, such as modular power sources, energy storage systems for batteries with different states of charge, auxiliary power units for electric vehicles, laboratory test power supplies, and specific industrial drive systems, can benefit from the suggested converter. Its ability to scale voltage levels without added hardware makes it well-suited for scenarios where efficiency, waveform quality, and expandability are essential.

CREDIT AUTHORSHIP CONTRIBUTION STATEMENT

Sathya Agila Sathish Chandar: conceptualization; methodology; investigation; writing – original draft.
Thiyagarajan Venkatraman: formal analysis; supervision; writing review & editing; validation.

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