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PERFORMANCE ENHANCEMENT STRATEGY FOR VOLTAGE-SOURCE INVERTERS USING W-TYPE CARRIER FUNCTION

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Keywords: Pulse width modulation (PWM); Modified carrier PWM; W-type carrier; Voltage source inverter; Field-programmable gate array (FPGA).

A new pulse-width modulation (PWM) switching approach has been introduced by modifying the carrier waveform, aiming to overcome the limitations of conventional methods for generating the fundamental component within the linear modulation range. This innovative technique is specifically designed for use in voltage-source inverters. Its effectiveness is evaluated by analyzing key performance metrics, such as the fundamental output voltage and Total Harmonic Distortion (THD), across a wide operating range. Extensive simulation studies have confirmed that the proposed PWM method offers notable performance improvements over traditional schemes.

1. INTRODUCTION

Three-phase pulse-width modulation (PWM) strategies are the foundation for controlling voltage-source inverters (VSIs) used in electric drives, renewable energy conversion, and smart grid systems. These methods generate desired AC output voltages from DC sources by adjusting the switching patterns of high-frequency switching devices, improving power quality, system efficiency, and dynamic performance. The traditional sinusoidal PWM (SPWM) and space vector PWM (SVPWM) methods remain predominantly used for their enhanced output characteristics, simplicity, and reliability. The SVPWM method facilitates improved DC bus voltage utilization and reduced harmonic distortion compared to SPWM [1–3]. To address the enhancement in improving the performance indices, several research avenues have focused on developing advancements in PWM techniques, which include model predictive PWM (MPPWM), Discontinuous PWM (DPWM), and hybrid PWM methods. MPPWM has gained more interest for enabling fast dynamic response and optimizing multiple control objectives in real time, particularly under wide variation in load conditions [4–6]. DPWM techniques have been formulated to reduce switching losses by clamping specific phases during certain intervals [7,8]. In multilevel and modular inverter systems, hybrid PWM methods that amalgamate low-frequency fundamental modulation with high-frequency PWM enable reduced switching losses and improved harmonic performance [9–11]. Carrier-based and carrier-less techniques have also been explored for cascaded H-bridge and flying capacitor inverters [12,13]. Other variants in PWM strategies, such as digital control strategies using FPGA and DSP implementations, provide real-time PWM generation with improved flexibility and control accuracy [14,15]. The primary outcome of this method is to achieve a higher fundamental voltage, typically seen in overmodulation, while working within the linear modulation region. On the other hand, the strategy focuses on reducing THD and attenuating the impact of dominant lower-order harmonics, which are significant impediments in inverter circuits.

2. PRINCIPLE OF THE W-TYPE CARRIER TECHNIQUE

The phenomenon of carving a new carrier signal from a traditional triangle carrier wave is shown in Fig. 1. The proposed carrier is derived from the traditional triangle carrier by grouping two adjacent triangles, which are inverted by 180° to follow the symmetry in its shape.

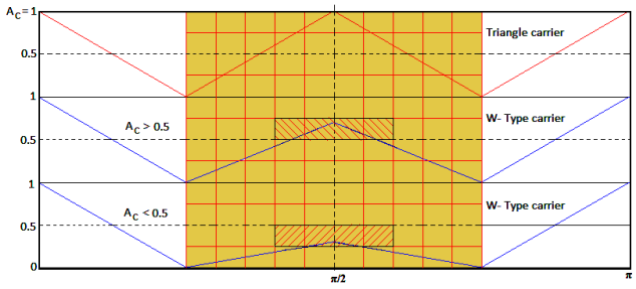


Fig. 1 – Proposed W-type carrier.

The right sector of the first triangle and the left sector of the triangle waves are grouped to form the apex point of the proposed W-type carrier. The traditional PWM technique is composed of a symmetrical triangle carrier, followed in sequence to form a carrier band. The triangle carrier is compared with a reference sine to produce PWM pulses to drive the switches of the PWM inverter. The output voltage of the PWM inverter is varied proportionally to the duty cycle of the pulses applied to the PWM inverter, as shown in Fig. 2. To understand the behavior of traditional triangle carrier PWM, the width of the pulse is varied proportionally to the area under the sine wave during the instant, and it inhibits the characteristics of the fundamental sine. The pulse number is determined by the number of triangles per half cycle of the fundamental sine, and it is (mf±1), where 'mf' is the frequency modulation index. Increasing the carrier wave's switching frequency reduces the harmonic content of the output voltage, resulting in greater power loss and a lower output voltage in the linear modulation region. With this perspective, a novel carrier signal, namely the 'W' type carrier, is formulated to increase the output fundamental voltage and reduce the THD over a wide operating region.

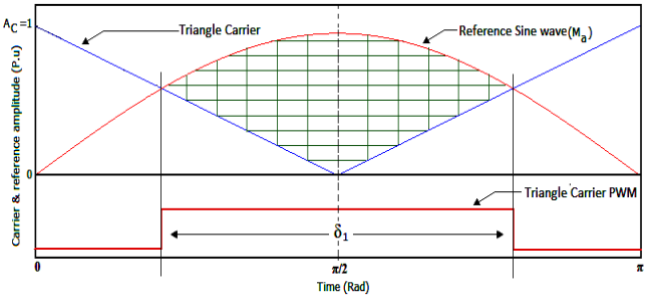


Fig. 2 – Variation of pulse width for higher modulation depth in conventional triangle PWM.

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It is inferred from Figs. 2 and 3 that the pulse width is widened ($\delta_2 > \delta_1$) for the same modulation depth, which implies the output voltage is proportionally increased over the modulation range in the case of W-type carrier PWM.

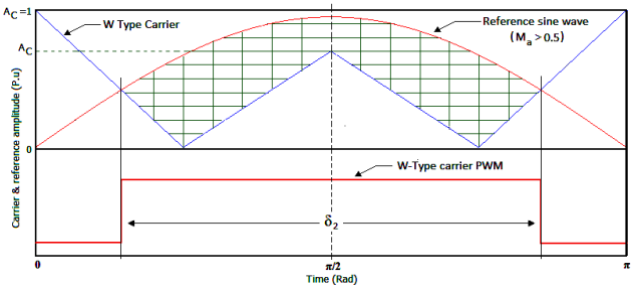


Fig. 3 – Variation of pulse width for higher modulation depth in the proposed W-type carrier PWM.

At low modulation index, the pulse train width increases, leading to greater switching and a higher output voltage than with the traditional triangle carrier, as depicted in Fig. 4.

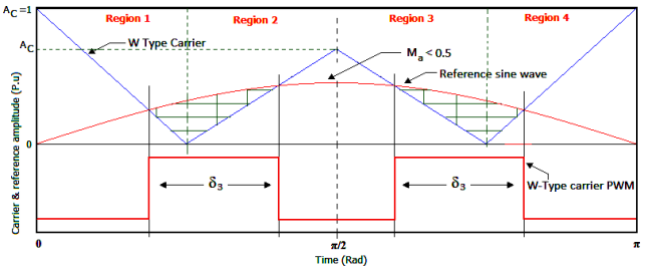


Fig. 4 – Variation of pulse width for lower modulation depth in proposed W-type carrier PWM.

The pulse width for the i^{th} pulse in the pulse train is obtained as $\delta_i = \theta_{2i} - \theta_{2i-1}$ shown in Table 1.

Table 1

Mathematical equation for the carrier function and the angle of intersection.

Region	Mathematical equation for each region Fig. 4	Switching instants with reference sine $V_r(\theta) = M_a \sin\theta_i$	Interval
1	$V_C(\theta) = 1 - \left(\frac{4M_f}{\pi}\right)\theta$	$M_a \sin\theta_i = \left(1 - \left(\frac{4M_f}{\pi}\right)\theta_i\right)$	$0 \le \theta \le \left(\frac{\pi}{4M_f}\right)$
2	$V_C(\theta) = A_C\left[\left(\left(\frac{4M_f}{\pi}\right)\theta\right) - 1\right]$	$M_a \sin\theta_i = A_C\left[\left(\left(\frac{4M_f}{\pi}\right)\theta_i\right) - 1\right]$	$\left(\frac{\pi}{4M_f}\right) \le \theta \le \left(\frac{\pi}{2M_f}\right)$
3	$V_C(\theta) = A_C\left[1 - \left(\frac{4M_f}{\pi}\right)\left(\theta - \left(\frac{\pi}{2M_f}\right)\right)\right]$	$M_a \sin\theta_i = A_C\left[1 - \left(\frac{4M_f}{\pi}\right)\left(\theta_i - \left(\frac{\pi}{2M_f}\right)\right)\right]$	$\left(\frac{\pi}{2M_f}\right) \le \theta \le \left(\frac{3\pi}{4M_f}\right)$
4	$V_C(\theta) = \left(\frac{4M_f}{\pi}\right)\left[\theta - \left(\frac{3\pi}{4M_f}\right)\right]$	$M_a \sin\theta_i = \left(\frac{4M_f}{\pi}\right)\left[\theta_i - \left(\frac{3\pi}{4M_f}\right)\right]$	$\left(\frac{3\pi}{4M_f}\right) \le \theta \le \left(\frac{\pi}{M_f}\right)$

The duty cycle of the PWM pulse can be calculated as $D = \frac{\sum_{i=1}^{N_P}\delta_i}{\pi}$. The harmonic content of the inverter output voltage is evaluated using the Fourier coefficients $a_n = \left(\frac{2V_{dc}}{n\pi}\right)\sum_{i=1}^{N_P}(\sin(n\theta_{2i}) - \sin(n\theta_{2i-1}))$ $b_n = \left(\frac{2V_{dc}}{n\pi}\right)\sum_{i=1}^{N_P}(\cos(n\theta_{2i}) - \cos(n\theta_{2i-1}))$. The magnitude of the nth harmonic is $V_n = \sqrt{(a_n)^2 + (b_n)^2}$. The fundamental component corresponds to $n = 1$, $V_1 = \sqrt{(a_1)^2 + (b_1)^2}$, where M_f and A_C are the frequency modulation index and carrier amplitude scaling factor.

3. ANALYSIS OF SWITCHING (T_{ON} AND T_{OFF})

The apex point plays an important role in determining the pulse width and the number of pulses in the pulse sequence. It is essential to understand the behavior of the proposed carrier by varying the apex value over (0 to 1) during PWM modulation with the reference sine wave. An examination is required to carry out to understand the concept by choosing the apex value of the proposed carrier above or below 0.5, as shown in Fig. 1. With the proposed W-Type carrier PWM, the number of switching (TON or TOFF) per fundamental switching cycle should be reduced over the broad modulation depth to achieve reduced switching loss. In this study, the proposed carrier PWM is tested in a 3- level inverter with the apex point lying above and below 0.5 to examine the switching number per fundamental cycle.

3.1 CARRIER APEX VALUE AS 0.7 AND ($0 < M_a < 1$)

To understand the behavior of the proposed W-type carrier PWM, it is necessary to choose the carrier frequency for both methods to be the same and switch at different modulation indices. The switching frequency taken for the study is 1 kHz, and the modulation index is taken from the range between 0.5 and 1. For the modulation index of 0.95, all the carriers are intersected by the reference sine in both the Triangle carrier and the W-Type carrier methods, as shown in Fig. 5.

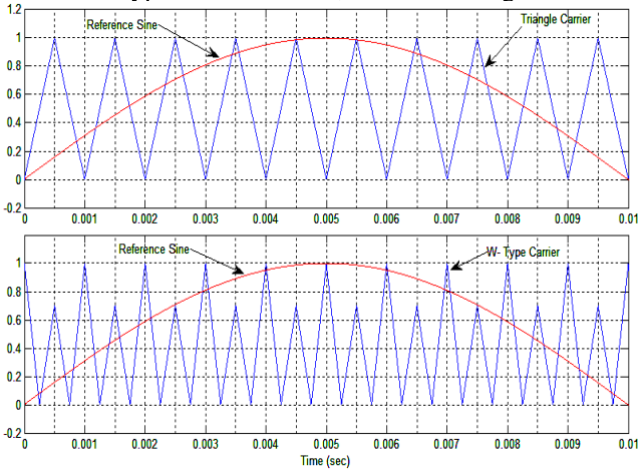


Fig. 5 – Behavior of proposed PWM with ($A_C = 0.7$) and ($M_a = 1$).

The area of all the carriers under the intersections contributes to the output voltage. The number of switches in the W-Type carrier is doubled due to more intersections near the apex of the W-Type carrier since the apex value is closer to 1. At higher modulation depths, the number of switches is constant in the proposed carrier with a wider pulse width than in triangle-carrier PWM, as seen in Fig. 8 (Subsection 3.1).

3.1 CARRIER APEX VALUE AS 0.3 AND ($0 < M_a < 1$)

For the modulation index of 0.4, all the carriers are intersected by the reference sine in both the Triangle carrier and the W-type carrier methods, as shown in Fig. 6. The area of all the carriers under the intersections contributes to the output voltage. The number of switches in the W-type carrier is slightly higher by 2 than in traditional triangle PWM, with an apex value of 0.3, as shown in Fig. 6 to 8, the pulse

number is proportional to (Mf), with a wider pulse width, as discussed in the classical triangle PWM.

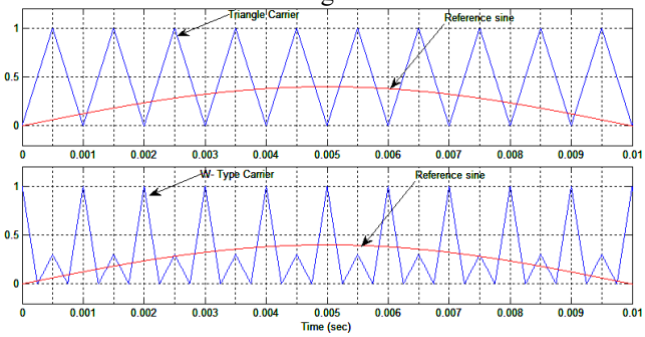


Fig. 6 – Behavior of proposed PWM with (A_C = 0.3) and (M_a = 0.4).

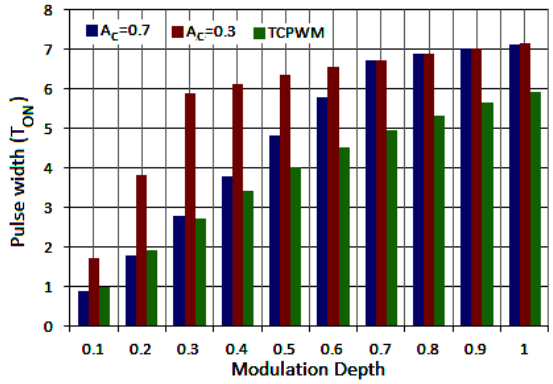


Fig. 7 – Variation of pulse width against modulation depth.

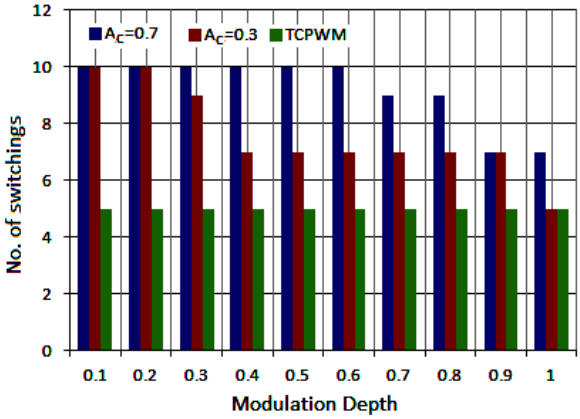


Fig. 8 – Variation of pulse number against modulation depth.

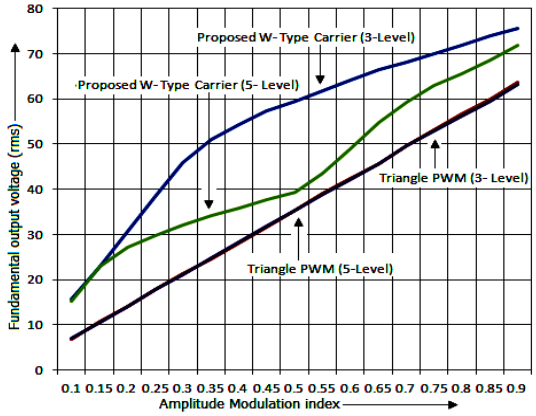


Fig. 9 – Variation of fundamental output voltage against modulation index.

Figures 9 to11 demonstrate that the proposed W-type carrier PWM improves the fundamental RMS output voltage while reducing total harmonic distortion and power loss compared with the conventional triangular carrier PWM. These improvements are achieved through carrier-wave shaping alone, without additional control complexity or hardware.

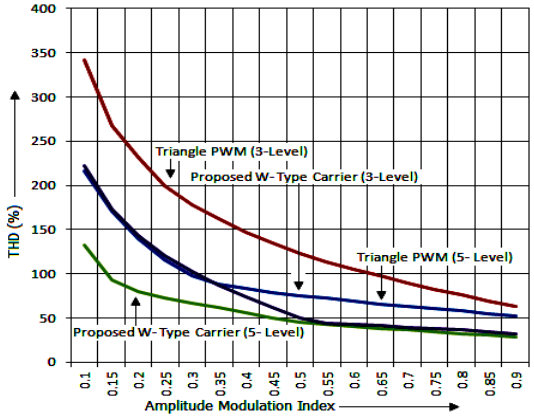


Fig. 10 – Variation of THD against modulation index.

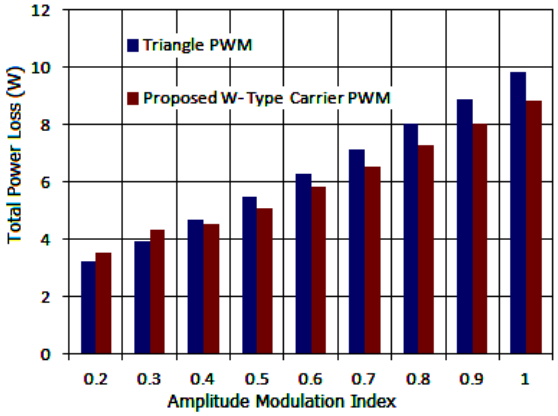


Fig. 11 – Variation of total power loss against modulation index.

4. PERFORMANCE ANALYSIS IN VSI

From the preceding discussion, it is concluded that the apex point is fixed below 0.5 to get a better output voltage profile with lower THD by compromising a slight increase in pulse number with low switching frequencies. The performance of the new W-type carrier is examined in single-phase 3-level and 5-level inverters and three-phase inverters. The study used MATLAB/Simulink to understand the operating characteristics of the proposed carrier function. The input parameters for the case study are V_{dc} = 100V, switching frequency (f_s) = 1 kHz, and modulation depths of 0.8 and 0.3. The resistive-inductive load is considered for study, with R = 100 Ω and L = 150 mH.

4.1 THREE-LEVEL VSI

The PWM pulses are obtained by direct comparison of the triangle carrier, W-Type carrier, and reference sine wave using relational operators in MATLAB/Simulink. The output voltage and its voltage spectrum for both methods are presented in Figs. 12 and 13, respectively. To reduce power loss, a fundamental switching logic operator [15–23] is embedded in the proposed W-type carrier PWM generation to switch high-frequency switching devices. The logical circuitry is portrayed in Fig. 14 to understand the switching operation in single-phase inverters. The method uses three square wave signals (F,Q,C) with frequencies of the fundamental frequency (f_o), ($2f_o$), and (f_o/2), and base PWM

pulses (P1 and P2) obtained from the PWM generator. The square wave frequencies ($2f_o$) and ($f_o/2$) toggle the PWM per quarter and full cycles to reduce the switching loss. Therefore, the power loss is balanced over two cycles of the fundamental frequency in all the devices. The PWM pulses and output voltage are shown in Fig. 15. The load voltage, along with the voltage spectrum for a 5-level inverter, is presented in Fig. 16. The line voltage for a three-phase inverter using W-Type carrier PWM is shown in Fig. 17.

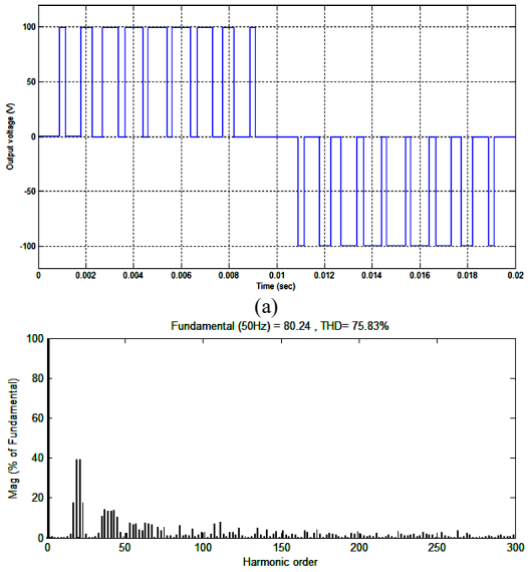


Fig. 12 – (a) Output voltage (b) Voltage spectrum for triangle carrier PWM.

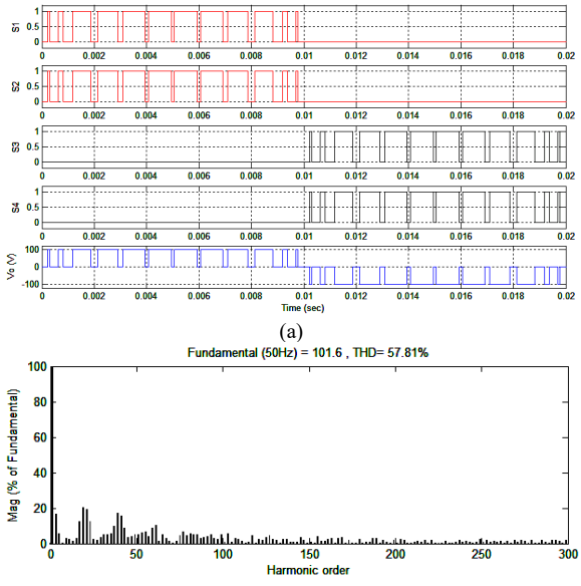


Fig. 13 – (a) Pulse pattern and output voltage; (b) Voltage spectrum for the proposed W-type carrier PWM.

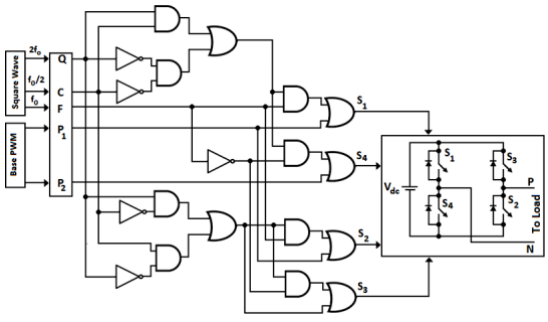


Fig. 14 – Logical circuitry for the PWM generation using W-type carrier.

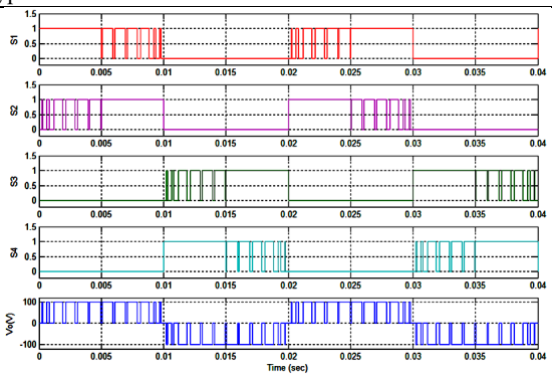


Fig. 15 – PWM pulses and output voltage using the PWM methodology.

4.2 FIVE LEVEL VSI

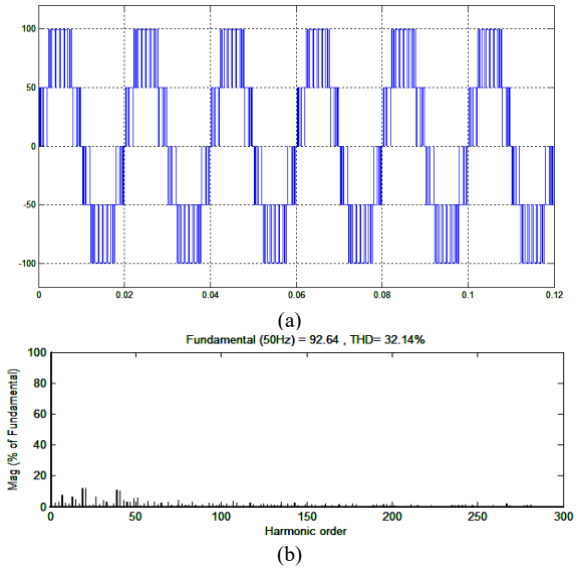


Fig. 16 - (a) Load voltage (b) Voltage spectrum for 5- level inverter.

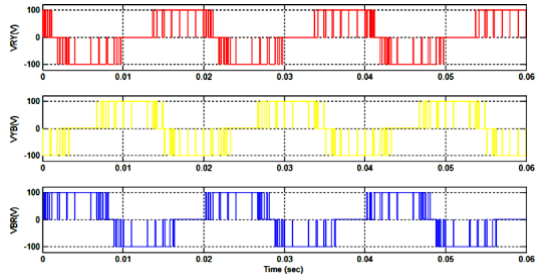


Fig. 17 – Line voltages for a three-phase inverter.

4.3 THREE-PHASE INVERTER

5. EXPERIMENTAL INVESTIGATIONS

The practical feasibility of the proposed W-type carrier PWM is demonstrated in an FPGA controller with an input voltage of 150V and a switching frequency of 1 kHz, M_a = 0.8, using the same load specifications. The experimental investigations have two folds with PWM generation for single-phase 3-level and 5- level inverters. The proposed W-Type carrier is generated in a Xilinx Spartan 3E FPGA controller using up/down counters. The counter's limits can be determined using the FPGA clock frequency. The clock frequency for the Xilinx Spartan 3E FPGA controller is 50 MHz. The reference sine wave is generated by taking 400 samples to compute instantaneous values and forming them as Look-Up Tables (LUTs). A VHDL code is written to fetch

the sine data from the memory and compare it with the W-type carrier to produce base PWM pulses. Three square signals of frequency 50 Hz, 100 Hz, and 25 Hz are generated using counters and flip-flops. To generate the desired pulse sequence for 3- and 5- level inverters, a behavioral model is used. The flow chart for the PWM generation methodology is shown in Fig. 18. A suitable VHDL block is developed to generate the PWM pulses without/with fundamental switching swapping for the single-phase 3-level inverter and is presented in Figs. 19 and 20, respectively. The output voltage for the 3- and 5-level inverters is portrayed in Figs. 21 and 22. The Pulse sequence for a 5-level inverter is shown in Figs. 23 and 24. The experimental results accord with the simulation results.

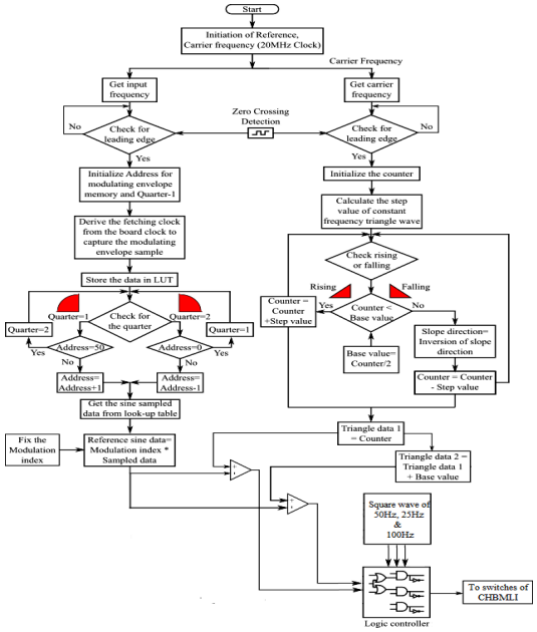


Fig. 18 – Flow chart for FPGA implementation of the proposed W-type carrier.

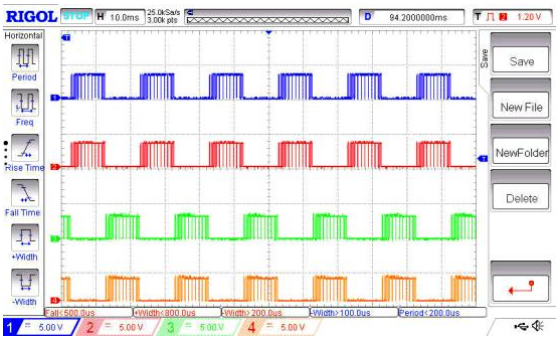


Fig. 19 – W-type carrier PWM without amalgamation of fundamental switching for a 3-level inverter.

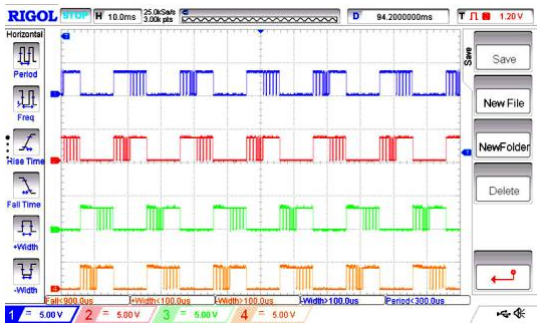


Fig. 20 – W-type carrier PWM with amalgamation of fundamental switching for a 3-level inverter.

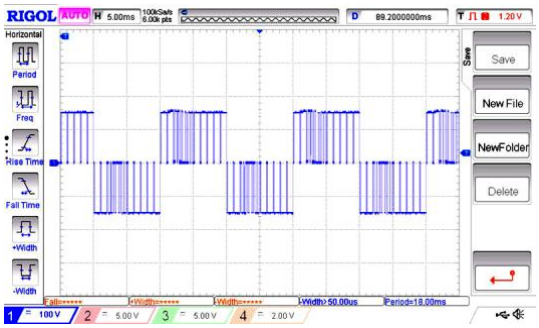


Fig. 21 – W-type PWM without amalgamation of fundamental switching for a 3-level inverter.

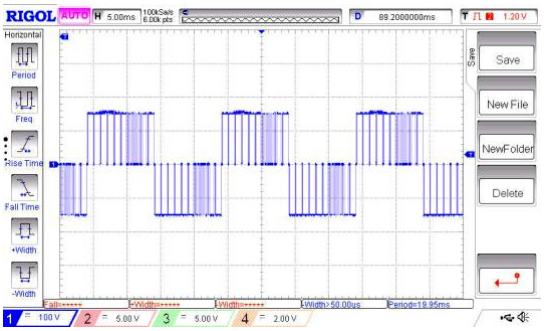
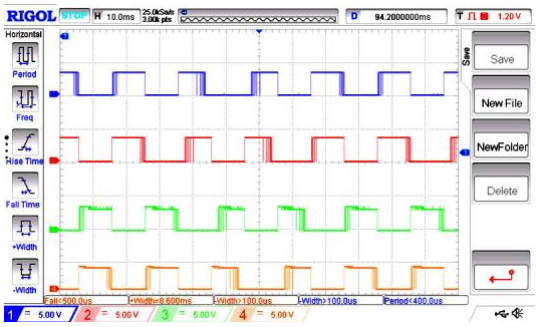
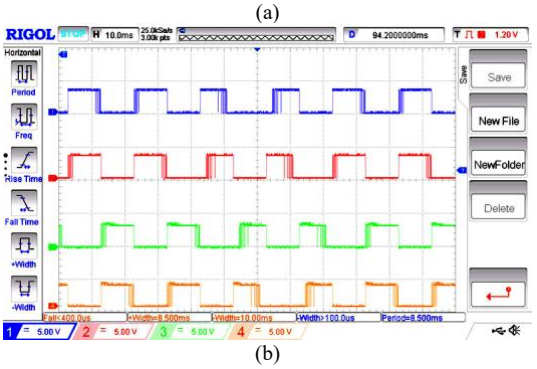


Fig. 22 – W-type PWM with amalgamation of fundamental switching for a 3-level inverter.



(a)



(b)

Fig. 23 – PWM pulses for 5- level inverter (a) H-bridge I (b) H-bridge II.

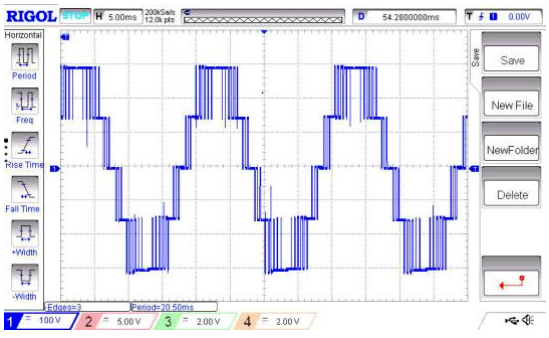


Fig. 24 – Output voltage for 5-level inverter.

6. CONCLUSION

The proposed modified W-type carrier method for VSI demonstrates significant improvements in the output voltage fundamental by altering the carrier shape and effectively reducing Total harmonic distortion (THD). This paves the way for improved power quality and increased efficiency in inverter operation. The strategy ensures a more uniform switching pattern and improved utilization of the DC link voltage across the full range of modulation depths. The adjustable carrier parameter (A_C) enables harmonic redistribution through systematic pulse-width control, while maintaining implementation complexity comparable to that of conventional carrier-based PWM. Simulation and experimental results confirm that the modified carrier achieves a significant improvement in harmonic performance over the conventional triangle PWM method, making it suitable for applications that demand high-quality voltage output and reliability.

CREDIT AUTHORSHIP CONTRIBUTION STATEMENT

Thamizharasan SANDIRASEGARANE: investigation, methodology, writing the original draft.

Saravanan SUBRAMANIAN: data curation; investigation; methodology; software; analysis; visualization; writing the original draft.

Arulvizhi ARULANANDHAN: resources; supervision; validation; writing review and editing.

Kamalakannan NANDHAGOPAL: supervision; validation; writing review & editing; references.

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REFERENCES

1. M. Mahbub, "Comparative analysis of five different PWM techniques on three-phase voltage source inverter-fed induction motor drive," 2021 2nd International Conference on Robotics, Electrical and Signal Processing Techniques (ICREST), Dhaka, Bangladesh, pp. 6–11 (2021).
2. Y. Shen, Y. Zhang, Z. Yin, G. Yuan, D. Xiao, H. Zhao, "Enhancing low carrier ratio induction motors with pulse pattern control for peak-to-peak torque ripple optimization," IEEE Trans. Transp. Electr., **11**, *5*, pp. 12236–12252 (2025).
3. J.S. Artal Sevil, R. Dufo López, J.L. Bernal Agustín, "Analysis of different PWM modulation techniques: comparison and design," 2018 XIII Technologies Applied to Electronics Teaching Conference (TAEE), La Laguna, Spain, pp. 1–8 (2018).
4. G.M. Gupta, S. Mondal, A.I. Maswood, "Model predictive control strategy of grid-tied converter control in weak grid conditions for containerized microgrid (CMG) systems," 2022 IEEE PES Innovative Smart Grid Technologies – Asia (ISGT Asia), Singapore, Singapore, pp. 364–368 (2022).
5. H. Le Huy, K. Slimani, P. Viarouge, "Analysis and implementation of a real-time predictive current controller for permanent magnet synchronous servo drives," IEEE Trans. Ind. Electron., **41**, *1*, pp. 110–117 (1994).
6. N. Gupta, S. Kumar, J.K. Saini, "Review of inverter control algorithms in grid-integrated solar photovoltaic system," 2020 Second International Sustainability and Resilience Conference: Technology and Innovation in Building Designs (51154), Sakheer, Bahrain, pp. 1–6 (2020).
7. H.B. Gobburi, V.B. Borghate, P.M. Meshram, "Discontinuous pulse width modulation techniques for modular multilevel converter," 2020 IEEE International Students' Conference on Electrical, Electronics and Computer Science (SCEECS), Bhopal, India, pp. 1–6 (2020).
8. H. Khan, E. Miliani, K. Drissi, "Evolutive discontinuous SVM for variable speed electric drive," Proceedings of the 2011 14th European Conference on Power Electronics and Applications, Birmingham, UK, pp. 1–7 (2011).
9. H. Jafari, D. Nazarpour, S. Golshannavaz, E. Babaei, "Design and analysis of a new hybrid three-phase multilevel inverter with improved specifications," 2021 29th Iranian Conference on Electrical Engineering (ICEE), Tehran, Iran, Islamic Republic of, pp. 258–262 (2021).
10. H. Jariwala, N. Shah, "Optimized modulation technique for cascaded H-bridge multilevel inverter," 2021 Innovations in Power and Advanced Computing Technologies (i PACT), Kuala Lumpur, Malaysia, pp. 1–6 (2021).
11. A. Routray, R.K. Singh, R. Mahanty, "Harmonic reduction in hybrid cascaded multilevel inverter using modified grey wolf optimization," IEEE Trans. Ind. Appl., **56**, *2*, pp. 1827–1838 (2020).
12. X. Zhao, D. Jiang, J. Chen, Z. Shen, Q. Li, "Leakage current suppression with capacitor voltage control of three-level flying capacitor grid-connected inverters," IEEE Trans. Ind. Electron., **69**, *3*, pp. 2191–2201 (2022).
13. M. Fukaya, T. Soeda, H. Haga, "A hybrid carrier-less dual inverter using a linear amplifier and a T-type inverter," 2025 Energy Conversion Congress & Expo Europe (ECCE Europe), Birmingham, United Kingdom, pp. 1–6 (2025).
14. P. Mishra, A. Banerjee, M. Ghosh, "FPGA-based real-time implementation of quad-rated digital PWM-controlled permanent magnet BLDC drive," IEEE/ASME Trans. Mechatronics, **25**, *3*, pp. 1456–1467 (2020).
15. P. Lakshmanan, P.A. Janakiraman, S.K. Ram, A. Abhishek, "FPGA-based digital control implementation of unbalance compensation in three-phase three-wire stand-alone inverters," 2022 IEEE 10th Power India International Conference (PIICON), New Delhi, India, pp. 1–5 (2022).
16. L.U. Sudha, J. Baskaran, S.A. Elankurisil, "FPGA techniques-based new hybrid modulation strategies for voltage source inverters," The Scientific World Journal, article 490151 (2015).
17. S. Thamizharasan, L.U. Sudha, J. Baskaran, S. Ramkumar, S. Jeevananthan, "Carrierless pulse width modulation strategy for multilevel inverters," IET Power Electron., **8**, pp. 2034–2043 (2015).
18. S. Thamizharasan, J. Baskaran, S. Ramkumar, S. Jeevananthan, "Cross-switched multilevel inverter using auxiliary reverse-connected voltage sources," IET Power Electron., **7**, pp. 1519–1526 (2014).
19. S. Thamizharasan, C. Krishnakumar, "Performance investigations of novel PWM control strategies for fundamental fortification in single-phase matrix converter for cyclo-conversion operation and FPGA implementations," Electric Power Components and Systems, **49**, *18–19*, pp. 1475–1488 (2022).
20. J. Thankaswamy, M. Paramasivan, M. Rathinam, U. Meenakshi Sundaram, "Chaotic randomized space vector pulse width modulation intended for induction motor drives in industrial applications: SVPWM for industrial motor drives," Rev. Roum. Sci. Techn. – Électrotechn. et Énerg., **69**, *4*, pp. 401–406 (2024).
21. A. Boudouda, A. Aibeche, A. Bouzida, N. Boudjerda, "A randomized carrier-based discontinuous pulse width modulation strategy for neutral point clamped three-level inverter," Rev. Roum. Sci. Techn. – Électrotechn. et Énerg., **69**, *3*, pp. 329–334 (2024).
22. S. Chennai, "Novel shunt active power filter based on nine-level NPC inverter using MC LSPWM modulation strategy," Rev. Roum. Sci. Techn. – Électrotechn. et Énerg., **69**, *1*, pp. 21–26 (2024).
23. M. Kaouane, M. Deroueche, N. Cherrat, A. Boukhelifa, "Study and design of a digital pulse width modulation signal generator for DC–DC converters," Rev. Roum. Sci. Techn. – Électrotechn. et Énerg., **71**, *1*, pp. 115–120 (2026).