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A NON-ISOLATED HIGH STEP-UP GAIN DC-DC CONVERTER WITH SWITCHED INDUCTOR AND VOLTAGE MULTIPLIER CELL

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Keywords: Continuous inductor current mode; DC-DC converter; Duty factor; Enhanced voltage gain; Grid-connected inverters; Reduced switch voltage and current stresses.

The grid-connected inverters require the DC power at high voltage only. The low-voltage DC power produced by the solar photovoltaic (PV) panels cannot be directly connected to the input of grid-connected inverters. Hence, a DC-DC converter is necessary to be installed as an interface between the solar PV panels' output and the grid-connected inverters. The interfacing DC-DC converter should have the capability to step-up the low DC voltage level of solar PV panels to the high DC voltage levels optimized to the grid-connected inverters. Such a high-voltage-gain DC-DC converter structure is proposed in this paper. The suggested non-isolated form of single-switch DC-DC converter topology can achieve relatively enhanced voltage gain at lower percentage of switch ON time itself by incorporating switched-inductors at the input side and a voltage multiplier cell at the output side of the converter. The topology has the additional advantage of reduced voltage and current stresses on the power switch and the diodes. The continuous inductor current mode operation of the converter is presented to validate the results of simulation of the converter at switch duty factor of 80%.

1. INTRODUCTION

Due to the global warming, environmental pollution, and day by day depletion of conventional energy sources, the alternate electrical power generation scenario makes use of the virtually inexhaustible renewable energy sources such as sun, wind, water, biomass, etc. The solar PV panels produce DC power at low voltage only. The grid-connected inverters require DC power at high voltage only. Hence, a power electronic interface is required between the solar PV panel's output and the inverter for stepping up the low voltage level of solar PV panels to high voltage level. Such a power electronic interface is called DC-DC converter with high step-up voltage gain. The high step-up DC-DC converters are classified into two forms such as (i). Transformer-free (non-isolated) structure tailored for medium power applications, and (ii). Isolated structure optimized for high power applications [1]-[9]. The work proposed in this paper involves non-isolated form of DC-DC converter.

A single-switch non-isolated DC-DC converter structure developed by integrating the traditional SEPIC and CUK configurations is suggested in [10], for the purpose of voltage gain improvement, where the Fractional Order PID (FOPID) controller is used for converter's dynamic performance improvement. For the duty cycle (k) value less than 40%, the converter structure suggested in [10] acts as a buck converter. Some authors projected a high step-up gain DC-DC converter configuration that combines the boost and SEPIC structures with diode-capacitor circuit for reducing the voltage stress on semiconductor based components [11]. The steady state analysis and the prototype model results are presented in [11] for validating the converter's performance. The features of the converter introduced in [11] include single-switch, enhanced voltage gain, improved efficiency of the converter, reduced voltage stress on the power switch.

A novel buck-boost single-switch DC-DC converter is illustrated in [12]. This converter has relatively higher voltage gain for the duty cycle (k) value greater than 30% and reduced switch voltage stress compared to the conventional non-isolated DC-DC converters in the literature. The converter reported in [12] is suitable for renewable energy and fuel-cell applications. Both the theoretical and experimental validation of the converter is carried out in [12]. A CCM operated non-isolated DC-DC converter structure that combines the traditional boost and modified CUK configurations is presented in [13], where converter's steady state behavior and state space modeling are explored. A hybrid single-switch single-inductor based DC-DC boosting converter that has high voltage gain capability with wide regulation range, low voltage stress on components and high efficiency is outlined in [14]. The prototype converter results are presented to validate the performance of the converter [14].

An integrated non-isolated high step-up gain DC-DC converter structure comprising the traditional SEPIC and voltage-gain-boosted CUK configurations is suggested in [15]. The developed CCM operated DC-DC converter has reduced active and passive components, enhanced voltage gain, and reduced stress on semiconductor elements. The steady state analysis, the simulation and the experimental investigations are carried out for the converter [15]. An integrated structure of conventional boost and CUK can give enhanced voltage gain and low switch voltage stress as suggested by the authors in [16]. The experimental results are also provided to validate the performance of the presented CCM operated single-switch highly efficient hybrid converter in MATLAB/SIMULINK platform [16]. Some authors illustrated the non-isolated form of single-switch Zeta-Mahafzah converter structures in [17]. The salient features of the converters suggested in [17] are enhanced converter's steady state performance, improved reliability, reduced voltage stress on the semiconductor components, improved voltage conversion ratio at low duty factor itself, and capability of producing synchronized multiple DC output voltages.

There are certain high step-up gain capability configurations of DC-DC converters with switched inductors, switched capacitors, and voltage multiplier cells (VMC). The combination of switched capacitors and VMCs can be employed in DC-DC converters to produce enhanced voltage gain. But, the high value of charging current results in more percentage increase in power losses [18]-[23]. The DC-DC converter topologies with coupled-inductors can also achieve improved voltage gain that is obtained by proper turns ratio adjustment. However, it has the drawback that the input current has more amount of ripples [24]. The definite number of VMCs can be employed in interleaved boost converters with a view to achieve enhanced voltage gain at

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low duty cycle itself [25].

The projected work in this paper explores a scheme for achieving the enhanced voltage conversion ratio using switched inductors at the source side and a voltage doubler cell at the load end of a non-isolated single-switch DC-DC converter. The proposed single-switch non-isolated DC-DC converter exhibits enhanced performance, primarily due to its higher voltage gain relative to comparable topologies presented in [10], [13], and [15]. The steady state analysis of the converter with relevant equivalent structures and equations is presented. The MATLAB/SIMULINK results of the converter are validated with the converter's theoretical performance. The proposed converter has certain merits such as the relatively improved voltage conversion ratio, decreased voltage stress on semiconductor components, and continuous inductor current.

The research presented in this paper has three important sections: The following section elucidates the operating performance of the converter during steady state and its voltage gain comparison with other non-isolated DC-DC converters in the literature. The next section depicts the converter's MATLAB/SIMULINK model and its results. The conclusion section summarizes the projected converter's key features.

2. THE MODES OF OPERATION OF THE PROJECTED NON-ISOLATED SINGLE-SWITCH DC-DC CONVERTER

This section provides the steady state analysis of the proposed non-isolated form of high step-up gain single-switch DC-DC converter operating in continuous inductor current mode. The converter's operating modes are analyzed with equivalent steady state converter structures, and inductor flux-balance equations that are used to derive the relationship between the output voltage (V_0) and the input voltage (V_{in}) in terms of the duty cycle ratio (k) of the converter.

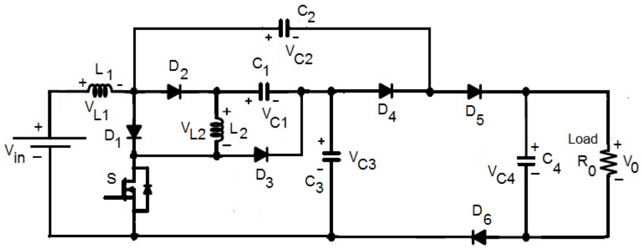

Fig. 1 - Proposed non-isolated high step-up gain DC-DC converter configuration

The power circuit configuration of the projected transformer free single-switch structure of DC-DC converter with enhanced voltage conversion ratio is depicted in Fig.1. The suggested converter topology ensures enhanced voltage gain (G_{CCM}) without extreme duty factor (k) due to the incorporation of switched inductor and voltage multiplier cell in the structure. The switched inductor cell consists of the inductors (L_1 and L_2), the diodes (D_1, D_2, and D_3), and the capacitors (C_1 and C_2) respectively. The voltage multiplier cell consists of the components such as D_4, D_5, D_6, C_3, and C_4 respectively. The ideal performance of the power MOSFET switch S, the inductors L_1 and L_2, the capacitors C_1, C_2, C_3, and C_4, and the diodes D_1, D_2, D_3, D_4, D_5, and D_6 is considered for the converter analysis. A DC source of 24 V is applied to the converter circuit. The converter's DC output voltage appears across a load resistor R_0. During the steady state operation of the converter, all the semiconductor based components experience relatively decreased voltage and current stresses. The operating principle of the suggested converter structure during the ON period and the OFF period of the power MOSFET switch S is explored as illustrated below.

The operation of the converter during Mode-I is explained with the help of the equivalent converter structure as shown in Fig.2. A PWM signal of suitable pulse width (T_{ON}) and switching frequency (f_s) is used to turn the power MOSFET switch S into conducting state. Accordingly, the duty factor ($k = T_{ON} / T_s$) can be set at any desired value. In this work, the typical variation of duty factor (k) is chosen in the range of 60% to 90%. The conducting switch S acts as short circuited path. The forward biasing of the diodes D_1 and D_3 makes them to conduct. The reverse biasing states of the diodes D_2, D_4, D_5 and D_6 make them to act as open circuited paths. The inductors L_1 is charged by the input voltage V_{in}. The capacitor voltage V_{C1} appears across the inductor L_2. All the capacitors keep their previously stored charges. The capacitor voltage V_{C4} supplies the load R_0. The two inductor voltages are expressed as Eq. 1.

$$V_{L1} = V_{in} \quad ; \qquad V_{L2} = V_{C1} \tag{1}$$

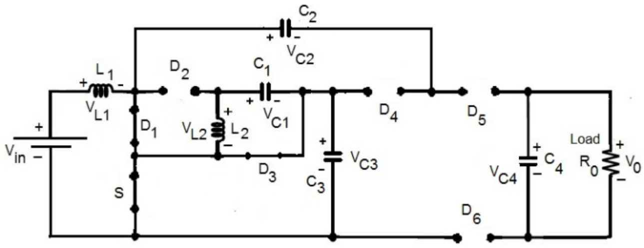

Fig. 2 – Converter structure during Mode-I operation

The converter's equivalent structure during Mode-II operation is as illustrated in Fig.3. The power MOSFET switch S is now acting as open circuited path due to its turn OFF condition. The diode D_1 acts as open circuit due to its reverse biased condition. The diode D_3 remains in conducting mode. The remaining diodes D_2, D_4, D_5, and D_6 are now in forward biased condition and hence they start to conduct. The energy stored in the inductors L_1 and L_2 charges all the capacitors and feeds the load. The inductor voltages are expressed as Eq. 2.

$$V_{L1} = V_{in} - V_{C1} \quad ; \qquad V_{L2} = V_{C1} \tag{2}$$

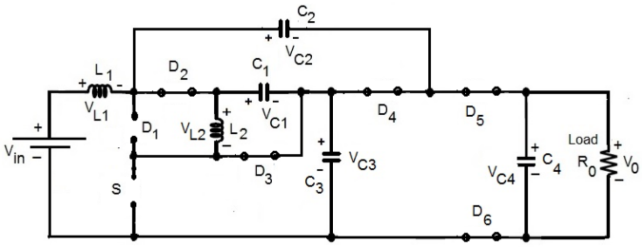

Fig. 3 – Equivalent structure during Mode-II operation of the topology

The flux-balance principle is applied to the inductors L_1 and L_2 for deducing the voltage gain (G_{CCM}) of the proposed converter using the Eq. 1 and 2. The following flux-balance equation is written as Eq. 3.

$$V_{in}kT_s + (V_{in} - V_{C1}(1-k)T_s = 0 \tag{3}$$

From Eq. 3, the capacitor voltage V_{C1} is obtained as Eq. 4.

$$V_{C1} = \frac{V_{in}}{(1-k)} = V_{C2} \tag{4}$$

The capacitor voltage V_{C3} is obtained as Eq. 5.

$$V_{C3} = V_{C1} + V_{C2} = \frac{2V_{in}}{(1-k)} \tag{5}$$

During turn OFF time of the power MOSFET switch S, the converter output voltage V_0 is expressed as Eq. 6.

$$V_0 = V_{C1} + V_{C2} + V_{C3} = \frac{4V_{in}}{(1-k)} \tag{6}$$

Hence, the expression for voltage gain (G_{CCM}) of the proposed converter is derived as Eq. (7).

$$G_{CCM} = \frac{V_0}{V_{in}} = \frac{4}{(1-k)} \tag{7}$$

It is obvious from the above Eq. 7 that the projected non-isolated high step-up gain converter can achieve four times the voltage gain of the conventional boost converter for the same value of duty factor (k). The voltage gain (G_{CCM}) and component count of the proposed converter are also compared with that of other structures of non-isolated form of high step-up gain DC-DC converters in the literature as illustrated in Table 1, which proves that the suggested converter has relatively enhanced voltage gain.

Table 1

Comparison of voltage gain and component count for the converters

Non-isolated Converters	Voltage gain (G_{CCM}) formula in CCM	Component count		
		Switches	Diodes	Passive components
Conventional boost converter	$\frac{1}{1-k}$	1	1	2
[10]	$\frac{2k}{1-k}$	1	2	7
[11]	$\frac{3+k}{2(1-k)}$	1	4	6
[12]	$\frac{3k}{1-k}$	1	3	10
[13]	$\frac{2+k}{1-k}$	1	4	7
[14]	$1+\frac{2n}{k}$	1	4	5
[15]	$\frac{k}{(1-k)^2} + \frac{k}{(1-k)}$	2	4	8
[16]	$\frac{1+k}{1-k}$	1	2	5
[17]	$\frac{2k}{1-k}$	1	2	7
Proposed	$\frac{4}{1-k}$	1	6	6

3. SIMULATION OF THE PROPOSED CONVERTER IN MATLAB/SIMULINK PLATFORM AND ITS RESULTS

A MATLAB/SIMULINK model of the projected non-isolated high step-up gain single-switch DC-DC converter is developed and the corresponding simulation results are presented and validated at switch duty cycle k = 80% and switching frequency (f_s) of 30 kHz. The passive and the semiconductor based components of the converter are designed according to the specifications as mentioned in Table 2. The pulse generator block is used to generate the suitable PWM signal as shown in Fig.4, for triggering the power MOSFET switch S into conduction state. An input DC voltage source of 24 V is used to energize the converter as shown in Fig.5. The converter supplies power to a resistive load (R_0) of 300 Ω. The current delivered (I_{in}) by the source is shown in Fig.6. The inductor L_1 voltage (V_{L1}) and current (I_{L1}) waveforms are depicted in Fig.7 and Fig.8. The inductor L_2 voltage (V_{L2}) and current (I_{L2}) waveforms are shown in Fig.9 and Fig.10. The power MOSFET switch S is subjected to an average voltage stress of around 200 V and an average current stress of around 3.5 A at k = 80% as illustrated in Fig.11 and Fig.12. The capacitors C_1, C_2, C_3, and C_4 have their voltage and current waveforms as depicted in Fig.13, Fig.14, Fig.15, Fig.16, Fig.17, Fig.18, Fig.19, and Fig.20 respectively. The uncontrolled semiconductor devices such as D_1, D_2, D_3, D_4, D_5, and D_6 experience certain limited values of voltage and current stresses as illustrated in Fig.21 to Fig.32. For the given load resistor of 300 Ω and switch duty cycle k = 80%, the converter output voltage and hence the load voltage (V_0) is obtained as around 490 V as illustrated in Fig.33. The corresponding load current (I_0) is calculated as 1.63 A as depicted in Fig.34. A typical duty cycle (k) range of 60% to 90% is chosen for validating the performance of the projected converter in MATLAB/SIMULINK environment, and the V_0 and I_0 values are tabulated in Table 3 for the converter simulated in the above specified range of the duty cycle (k).

Table 2

Simulation parameters for the converter

Parameters	Symbol	Value
DC source voltage	V_{in}	24 V
	L_1	50 µH
Passive components (Inductors & Capacitors)	L_2	150 µH
	C_1	50 µF
	C_2, C_3, C_4	100 µF each
Load resistor	R_0	300 Ω
Switching frequency	f_s	30 kHz
Duty cycle of the MOSFET switch S	k	80%

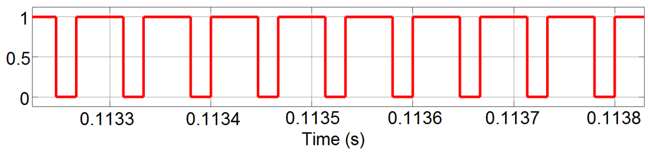

Fig. 4 – PWM signal applied to the power MOSFET switch S

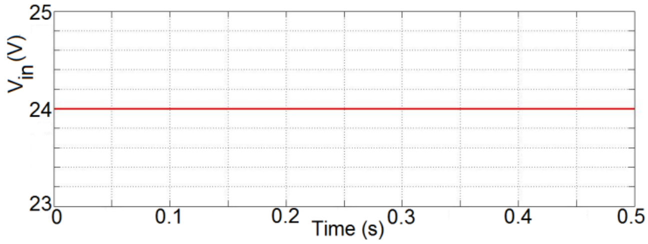

Fig. 5 – Input DC voltage applied to the proposed converter

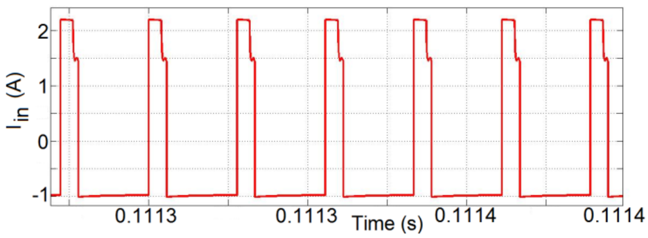

Fig. 6 – Input current (I_{in}) of the converter

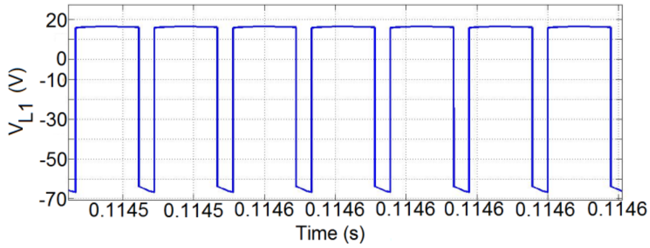

Fig. 7 – Voltage across the Inductor L_1 (V_{L1})

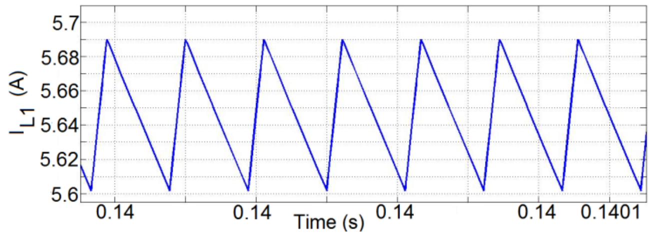

Fig. 8 – Current through the Inductor L_1 (I_{L1})

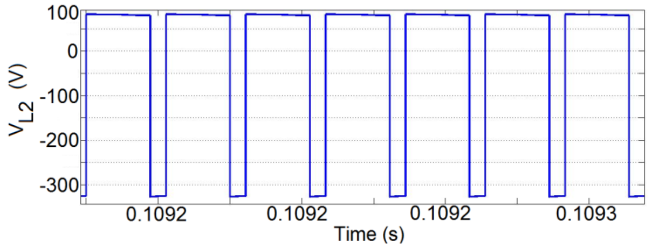

Fig. 9 – Voltage across the Inductor (V_{L2})

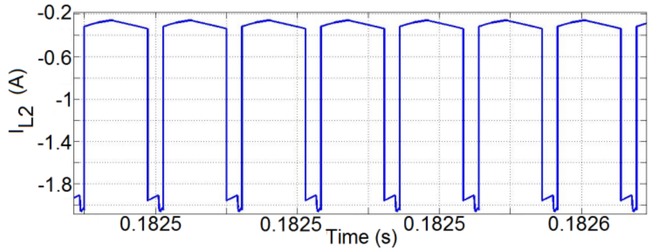

Fig. 10 – Current through the Inductor L_2 (I_{L2})

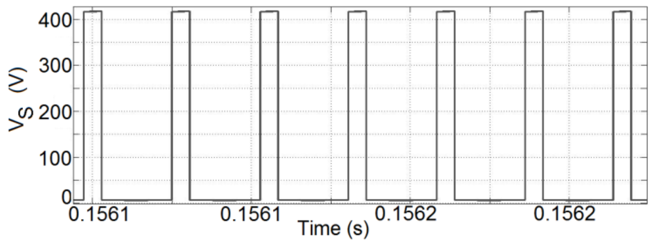

Fig. 11 – MOSFET switch voltage stress (V_S)

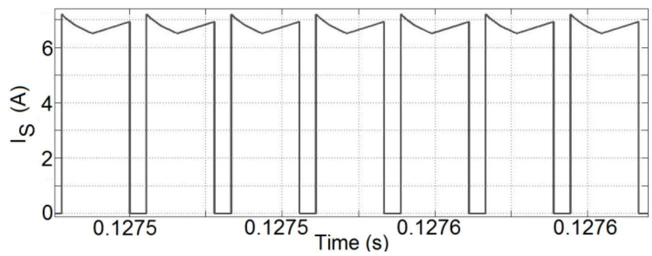

Fig. 12 – MOSFET switch current (I_S)

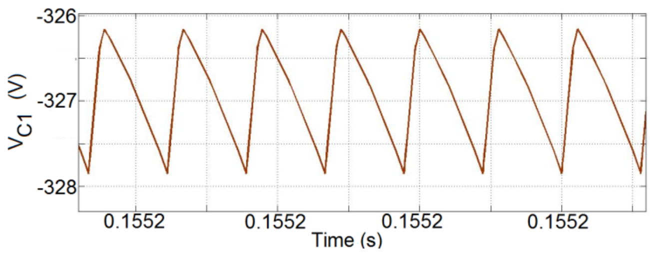

Fig. 13 – Voltage across the Capacitor C_1 (V_{C1})

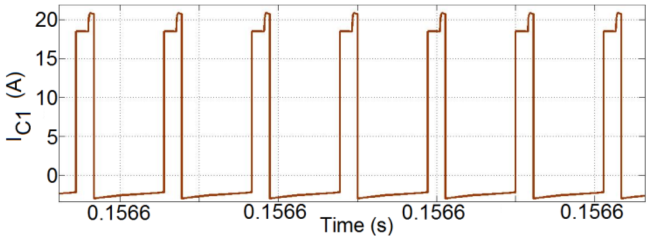

Fig. 14 – Current through the Capacitor C_1 (I_{C1})

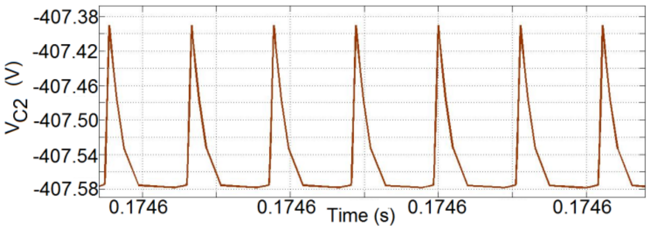

Fig. 15 – Voltage across the Capacitor C_2 (V_{C2})

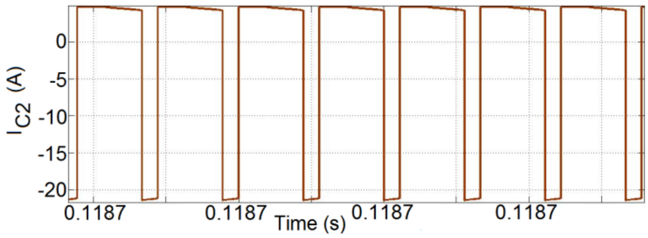

Fig. 16 – Current through the Capacitor C_2 (I_{C2})

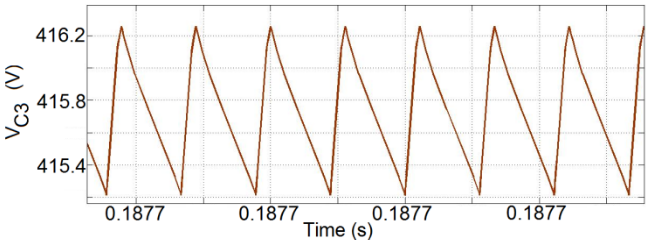

Fig. 17 – Voltage across the Capacitor C_3 (V_{C3})

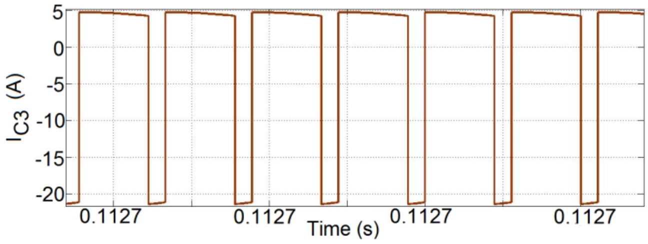

Fig. 18 – Current through the Capacitor C_3 (I_{C3})

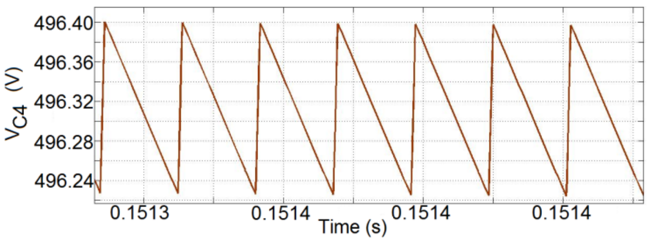

Fig. 19 – Voltage across the Capacitor C_4 (V_{C4})

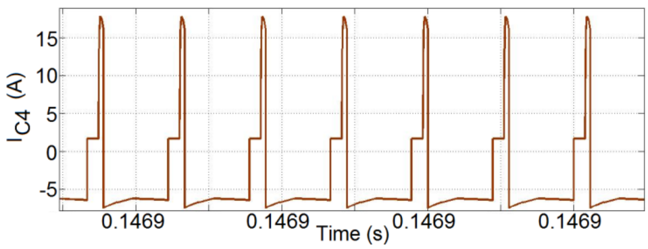

Fig. 20 – Current through the Capacitor C_4 (I_{C4})

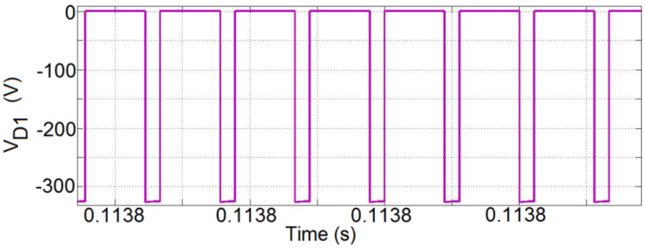

Fig. 21 – Voltage across the Diode D_1 (V_{D1})

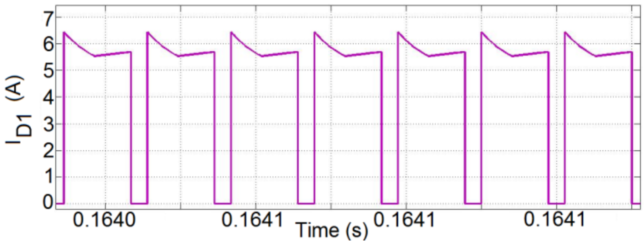

Fig. 22 – Current through the Diode D_1 (I_{D1})

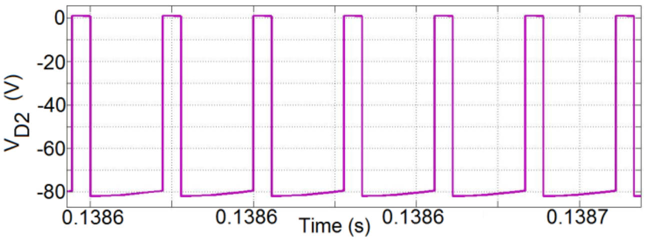

Fig. 23 – Voltage across the Diode D_2 (V_{D2})

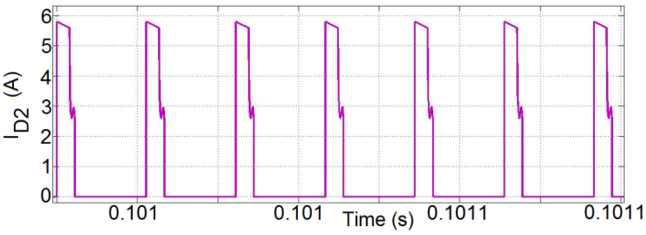

Fig. 24 – Current through the Diode D_2 (I_{D2})

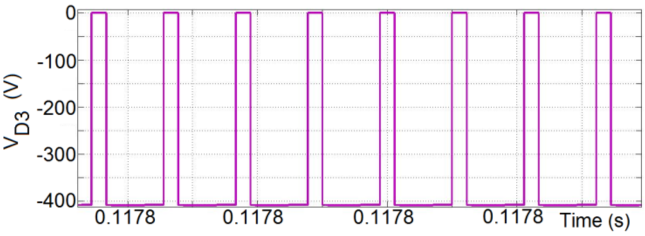

Fig. 25 – Voltage across the Diode D_3 (V_{D3})

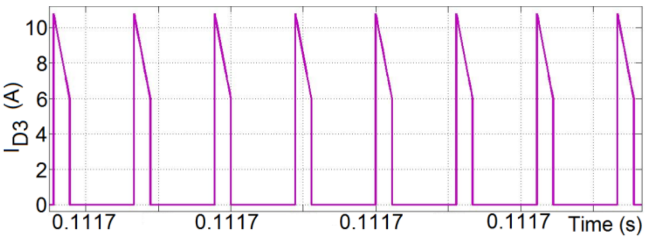

Fig. 26 – Current through the Diode D_3 (I_{D3})

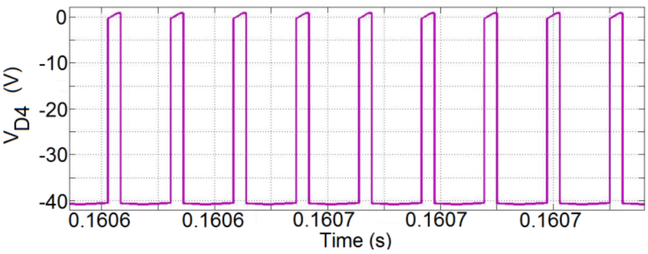

Fig. 27 – Voltage across the Diode D_4 (V_{D4})

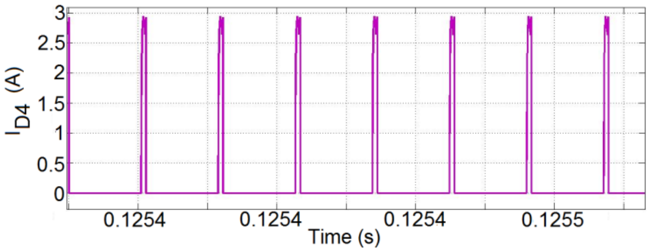

Fig. 28 – Current through the Diode D_4 (I_{D4})

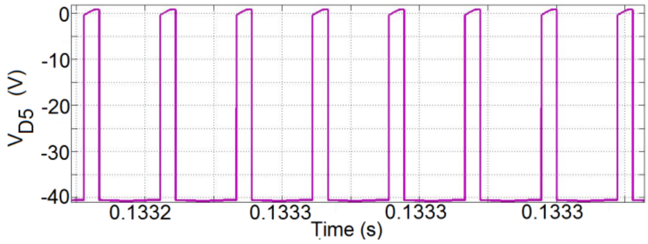

Fig. 29 – Voltage across the Diode D_5 (V_{D5})

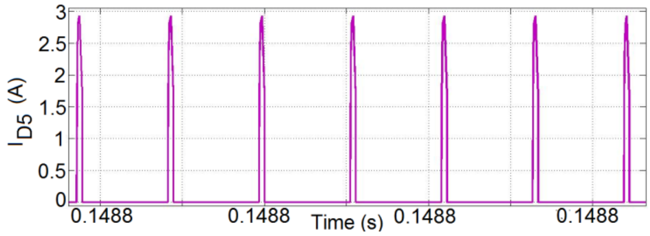

Fig. 30 – Current through the Diode D_5 (I_{D5})

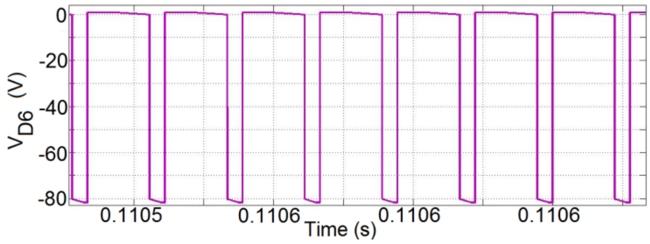

Fig. 31 – Voltage across the Diode D_6 (V_{D6})

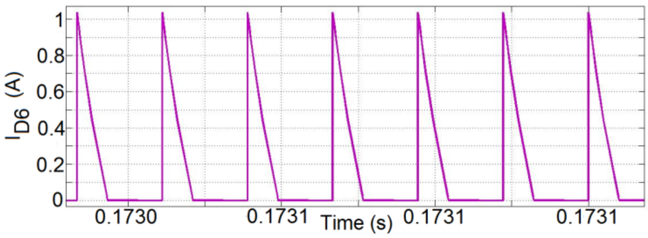

Fig. 32 – Current through the Diode D_6 (I_{D6})

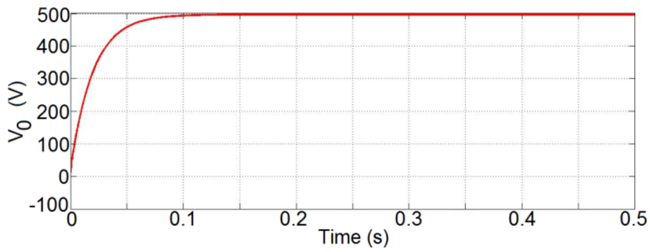

Fig. 33 – Output voltage (V_0)

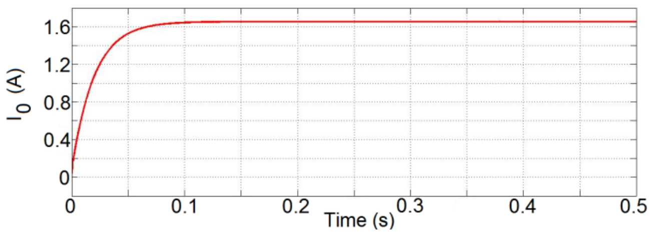

Fig. 34 – Output current (I_0)

Table 3
Load voltage (V_0) and load current (I_0) values

Duty cycle (k)	V_0 (V)	I_0 (A)
0.6	240	0.80
0.7	320	1.07
0.8	490	1.63
0.9	960	3.2

4. **CONCLUSIONS**

The research work projected in this paper explores the steady state behavior of a non-isolated high step-up gain DC-DC converter topology with switched inductor and voltage multiplier cell. The continuous conduction mode operation of the converter under ON and OFF states of the power MOSFET switch is analyzed by means of equivalent converter structures and flux-balance equations. The proposed single-switch converter structure with simple PWM control technique ensures relatively improved static voltage gain at lower value of switch duty cycle (k) itself due to the use of switched inductor based boost cell and voltage doubler structure, and relatively reduced voltage and current stresses on semiconductor based components. The performance of the converter is validated by simulating the converter setup energized by a 24 V DC source, in MATLAB/SIMULINK platform. The simulation waveforms of all active and passive components are analyzed at the switching frequency (f_s) of 30 kHz and 80% duty cycle of the converter supplying power to a 300 Ω resistive load. However, the lack of experimental validation is the limitation of the proposed work. The suggested high step-up gain DC-DC converter can be employed for boosting the low voltage level of solar PV panels to high voltage levels. Also it finds applications in EV (Electric Vehicle) technology and DC microgrids that can supply power to DC loads.

CREDIT AUTHORSHIP CONTRIBUTION STATEMENT

Murali D: Methodology; Conceptualization; Investigation; Experimental design; Writing – original draft; Validation.

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