Rev. Roum. Sci. Techn.– Électrotechn. et Énerg.
Vol. **71**, *3*, pp. 421–426, Bucarest, 2026

MONTE CARLO-BASED UNCERTAINTY ANALYSIS OF NON-IDEAL BIDIRECTIONAL DC-DC CONVERTER

AHMET GANI[1], SEZAI ALPER TEKIN [2]

Keywords: Monte Carlo simulation; Uncertainty analysis; Bidirectional DC-DC converter; Non-ideal converter.

Bidirectional DC-DC converters are widely employed in DC bus-based power systems that supply resistive DC loads due to their simple structure and inherent capability for bidirectional power flow. This paper presents a comprehensive Monte Carlo-based uncertainty analysis of a non-ideal bidirectional DC-DC converter operating with a resistive DC load. Inductor and capacitor tolerances, parasitic resistances, and component operating temperature uncertainties are simultaneously randomized to assess their combined impact on DC bus voltage regulation during bidirectional operation. Simulation results confirm that the bidirectional converter maintains stable operation and bounded performance dispersion under parametric uncertainties. The proposed framework provides a robustness-oriented evaluation methodology that complements conventional deterministic analysis for DC bus-interfaced power converters.

1. INTRODUCTION

DC bus architectures have become increasingly prevalent in modern power electronic systems, including DC microgrids [1]. In such systems, bidirectional converters (BDCs) play a key role by enabling regulated power exchange between interconnected DC subsystems while maintaining a stable DC bus voltage under varying operating conditions. Owing to their simple structure, low component count, high efficiency, and inherent bidirectional power-flow capability, classical non-isolated bidirectional converters remain among the most widely adopted solutions for DC bus applications supplying resistive DC loads [2].

The fundamental operating principles and steady-state voltage gain characteristics of classical bidirectional DC–DC converters under resistive loading conditions have been well established in the literature [3]. Early analytical studies established voltage conversion relationships under the assumptions of ideal components and continuous conduction mode (CCM) operation, thereby providing the theoretical foundation for DC bus voltage regulation [4]. Building upon these foundations, subsequent research has focused on improving voltage regulation accuracy, reducing output voltage ripple, and enhancing converter efficiency through voltage-mode and current-mode control strategies tailored for resistive DC load conditions [5]. As DC bus systems evolved toward higher power density and stricter voltage regulation requirements, several studies incorporated non-ideal effects-such as inductor winding resistance, capacitor equivalent series resistance (ESR), and semiconductor conduction losses-into converter models to more accurately capture practical operating behavior [6].

These investigations demonstrated that parasitic elements significantly influence DC bus voltage deviation, output voltage ripple, semiconductor voltage stress, and conversion efficiency, particularly when the converter operates at high duty ratios or under wide variations in resistive load conditions. However, most of these analyses relied on deterministic or nominal parameter values, which fail to adequately reflect the inherent variability introduced by manufacturing tolerances and component dispersion. [7]. To overcome the limitations of deterministic modeling, uncertainty analysis techniques have gained increasing attention in power electronics research. Monte Carlo-based uncertainty analysis has been successfully applied to unidirectional DC-DC converters supplying resistive DC loads, enabling probabilistic evaluation of output voltage ripple, efficiency degradation, and semiconductor stress variations under parametric uncertainties [8].

Despite these advances, the uncertainty analysis of classical bidirectional DC-DC converters operating in DC bus applications has received comparatively limited attention. Existing BDC studies largely neglect tolerance-induced uncertainties or rely on single-parameter sensitivity analyses, which are insufficient to capture the combined and interacting effects of multiple non-idealities on DC bus performance [9,10].

Therefore, a clear research gap exists in the comprehensive Monte Carlo-based evaluation of the uncertainty performance of classical bidirectional DC-DC converters supplying resistive DC loads. Addressing this gap is essential for reliability-oriented design and realistic performance assessment of DC bus-interfaced power converters.

In this paper, a Monte Carlo-based uncertainty analysis framework is proposed to evaluate the performance of a classical bidirectional DC-DC converter operating with a resistive DC load. The combined effects of passive component tolerances, parasitic resistances, and component temperature uncertainties are analyzed in terms of output voltage ripple and output voltage deviation.

The remainder of this paper is organized as follows. Section 2 describes the non-ideal BDC circuit topology and its operating principles. Section 3 details the proposed Monte Carlo-based simulation methodology. Section 4 defines the performance indices used for uncertainty evaluation and discusses the Monte Carlo simulation results. Finally, Section 5 concludes the paper and outlines directions for future work.

2. NON-IDEAL BDC CIRCUIT TOPOLOGY

The classical non-ideal bidirectional DC-DC converter (BDC) topology considered in this study consists of two controllable non-ideal MOSFET switches, one inductor including winding resistance, and input/output capacitors with equivalent series resistance (ESR). Bidirectional power flow is obtained by selectively activating the appropriate MOSFET switch, enabling the converter to operate in buck or boost mode without changing the circuit configuration. Figure 1 illustrates the non-ideal BDC topology.

[1] Department of Electrical and Electronics Engineering, Faculty of Engineering, Architecture and Design, Kayseri University, Kayseri, Turkey.
2 Faculty of Engineering, Department of Industrial Design Engineering, Erciyes University, Kayseri, Turkey.
E-mail: ahmetgani@kayseri.edu.tr, satekin@erciyes.edu.tr (correspondence)

DOI: 10.59277/RRST-EE.2026.3.14

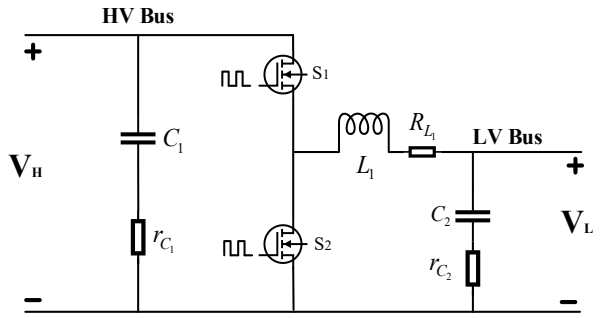

Fig. 1 – Non-ideal BDC circuit topology.

The converter operates in CCM under two fundamental operating modes.

Boost Mode: In this mode, switch S_2 enters conduction according to the duty cycle, whereas switch S_1 always remains off. Under ideal conditions, the steady-state voltage relationships are expressed as:

$$V_{H=}\frac{V_L}{1-D}. \quad (1)$$

As shown in Fig. 2, the non-ideal BDC operates in boost mode, transferring power from the low-voltage (LV) bus to the high-voltage (HV) bus.

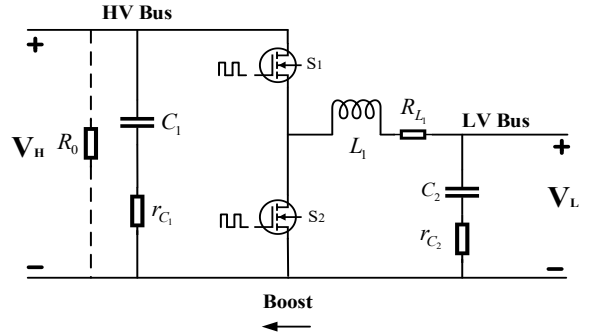

Fig. 2 – Boost mode of non-ideal BDC circuit topology.

Buck Mode: In this mode, switch S_1 conducts based on the duty cycle, while switch S_2 remains off. Under ideal conditions, the steady-state voltage relationships are expressed as:

$$V_{H=}\frac{V_L}{D}, \quad (2)$$

where D denotes the duty cycle [11], as shown in Fig. 3, the non-ideal BDC operates in reverse (buck) mode, transferring power from the HV bus to the LV bus.

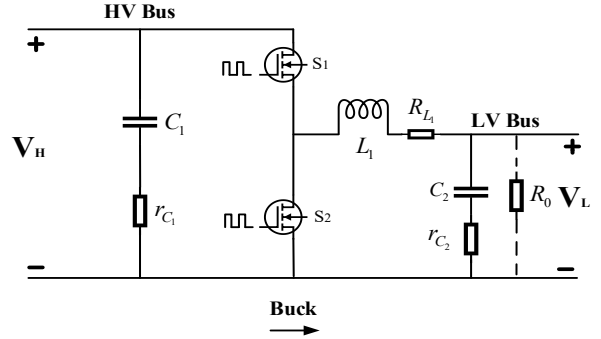

Fig. 3 – Buck mode of non-ideal BDC circuit topology.

3. MONTE CARLO-BASED SIMULATION

For manufacturing tolerances of non-ideal BDC converter, capacitors (C_1 and C_2) and equivalent series resistances ESRs (r_{C1} and r_{C2}); inductor L_1 and winding resistance (R_{L1}) and load resistance R_0 are modeled with manufacturing random tolerance deviations as follows [12]:

$$L'_1 = L_1\left(1+\delta_{L_1}\right), \quad (3)$$

$$C'_1 = C_1\left(1+\delta_{C_1}\right), \quad (4)$$

$$C'_2 = C_2\left(1+\delta_{C_2}\right), \quad (5)$$

$$R_{L'_1} = R_{L_1}\left(1+\delta_{R_{L_1}}\right), \quad (6)$$

$$ESR'_{C_1} = ESR_{C_1}\left(1+\delta_{C_1}\right), \quad (7)$$

$$ESR'_{C_2} = ESR_{C_2}\left(1+\delta_{C_2}\right), \quad (8)$$

$$R'_0 = R_0\left(1+\delta_{R_0}\right), \quad (9)$$

where δ terms represent random tolerance deviations, the circuit components of a non-ideal BDC with nominal and manufacturing tolerance values, both boost and buck modes, are given in Tables 1 and 2, respectively.

Table 1

Circuit components of a non-ideal boost mode BDC with nominal and manufacturing tolerance limits.

Components	Symbol	Nominal	Tolerance
Inductor	L_1	270 µH	20%
Winding resistance	R_{L_1}	0.0516 Ω	20%
Capacitors	$C_{1,2}$	220 µF	20%
ESRs	$r_{C_{1,2}}$	0.1133 Ω	20%
Input Voltage	V_L	12 V	-
Nominal Output Voltage	V_H	98 V	-
Load	R_0	50 Ω	5%
Switching frequency	f	20 kHz	-
Duty Cycle	D	0.89	-

Table 2

Circuit components of a non-ideal buck mode BDC with nominal and manufacturing tolerance limits.

Components	Symbol	Nominal	Tolerance
Inductor	L_1	270 µH	20%
Winding resistance	R_{L_1}	0.0516 Ω	20%

Circuit components of a non-ideal buck mode BDC with nominal and manufacturing tolerance limits.

Capacitors	$C_{1,2}$	220 µF	20%
ESRs	$r_{C_{1,2}}$	0.1133 Ω	20%
Input Voltage	V_L	12 V	-
Nominal Output Voltage	V_H	98 V	-
Load	R_0	1 kΩ	5%
Switching frequency	f	20 kHz	-
Duty Cycle	D	0.12	-

The flowchart for the Monte Carlo Simulation procedure of the non-ideal BDC is presented below. Figure 4 illustrates the workflow for the Monte Carlo-based uncertainty analysis of the non-ideal BDC converter. The analysis begins with the definition of the non-ideal converter model, which incorporates parasitic components such as inductor winding resistances and capacitor equivalent series resistances (ESRs) into the system model. Afterward, the nominal values and manufacturing tolerance ranges of the circuit

elements are assigned to represent the practical operating conditions encountered in real implementations.

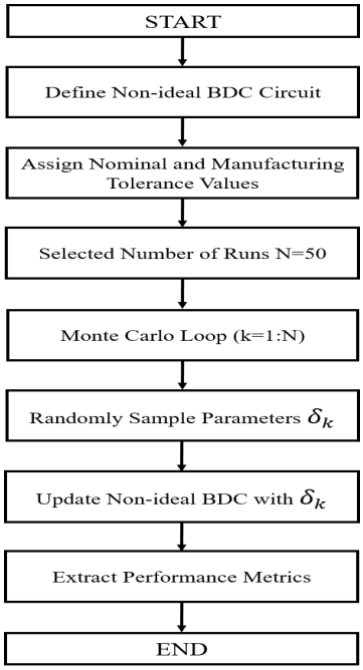

Fig. 4 – The flowchart of the Monte Carlo simulation procedure for the non-ideal BDC circuit.

Subsequently, the number of Monte Carlo iterations is determined ($(N = 50)$, and a stochastic simulation loop is initiated. During each iteration, the converter parameters are randomly sampled within their predefined tolerance intervals. These randomly generated uncertainty variables (δ_k) are then applied to the non-ideal converter model to update the circuit parameters dynamically [13,14]. Following the parameter update, the converter performance metrics, including output voltage ripple and output voltage deviation, are computed as follows:

Output Voltage Ripple: Typically expressed as the peak-to-peak value measured over one switching period around the nominal output voltage.

$$\Delta V_0 = V_{0,max} - V_{0,min}. \quad (10)$$

Output Voltage Deviation: The relative difference between the actual output voltage and its nominal value, used as a performance indicator to quantify voltage regulation accuracy under uncertain operating conditions.

$$\Delta \mathrm{V_d} = V_{0,max} - V_{0,nom}. \quad (11)$$

4. UNCERTAINTY EVALUATION

A detailed Monte Carlo Simulation procedure for the non-ideal BDC was performed in the LTspice Analog Devices simulation platform with component manufacturing and temperature uncertainties. The Monte Carlo simulation studies were performed using a PC with an AMD Ryzen 9 7900X processor at 4.7 GHz and 32 GB of RAM, with a sampling time of 0.1 µs. To ensure a fair evaluation across all scenarios, the total simulation time is set to 100 ms. The detailed modeling scenarios considered for the uncertainty evaluation of the non-ideal boost and buck modes of BDC are given in Table 3.

Table 3

Uncertainty evaluation of the non-ideal boost and buck modes of the BDC circuit.

Scenarios	Component Manufacturing Uncertainty	Component Temperature Uncertainty
Component Temperature Uncertainty Model	Fixed at nominal values	Temperature (℃) of $L_1, R_{L1}, C_1, C_2, r_{C1}, r_{C2}$, l varied within operating limits
Component Manufacturing Uncertainty Model 1	$L_1, R_{L1}, C_1, C_2, r_{C1}, r_{C2}$ varied within tolerance limits	Fixed at 25 (℃)
Component Manufacturing Uncertainty Model 2	R_0 varied within its tolerance limit	Fixed at 25 (℃)

Furthermore, the non-ideal inductor, capacitor, and resistor component technologies, along with their operating temperature range values, are provided in Table 4.

Table 4

Non-ideal inductor, capacitor, and resistance component technologies, along with their operating temperature ranges.

Components Technology	Operating Temperature Limits
C Würth Electronics Al Electrolytic	-25 to 105 ℃
PCV-2-274-10 / Coil craft	-55 to 150 ℃
R Vishay RCH Power Resistors	-55 to 125 ℃
AON2392 / MOSFET	-55 to 150 ℃

4.1 COMPONENT TEMPERATURE UNCERTAINTY MODEL

This scenario incorporates various uncertainty temperature values of passive components $L_1, R_{L1}, C_1, C_2, r_{C1}, r_{C2}, R_0$ are set to -25℃, 0℃, 25℃, 50℃, 75℃ and 100℃, respectively. In contrast, passive component tolerances are set to nominal values, and the operating temperature of the AON2392/MOSFET model is set to 25 ℃. Figure 5 presents the effect of various uncertainty temperature values for passive components on the BDC, with the duty cycle fixed at D = 0.89 and D = 0.12 in boost and buck modes, respectively.

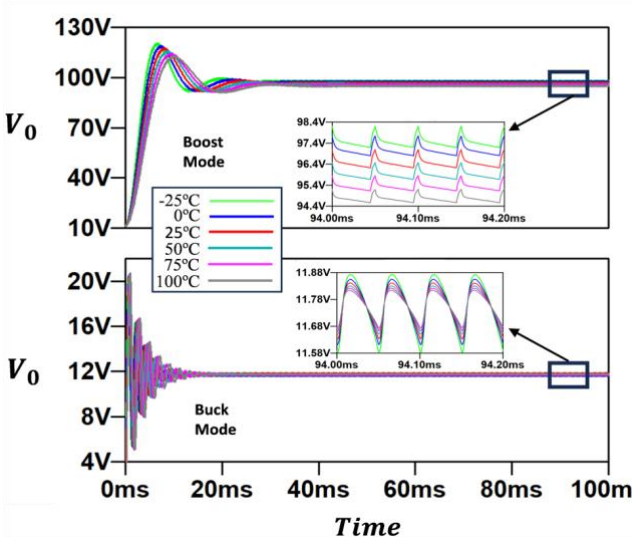

Fig. 5 – Effect of various uncertainty temperature values of passive components on the BDC with boost/buck modes.

The output voltage ripple and deviation results obtained from various temperature uncertainty values with boost mode are presented in Table 5.

Table 5

Output voltage ripple and deviation results obtained from various temperature uncertainty values with boost mode.

Temperature	Output Voltage Ripple	Output Voltage Deviation
-25 ℃	1.017 V	0.2 V
0 ℃	0.925 V	-0.268 V
25 ℃	0.849 V	-0.939 V
50 ℃	0.801 V	-1.523 V
75 ℃	0.724 V	-2.167 V
100 ℃	0.647 V	-2.791 V

As clearly indicated in Table 5, the minimum output voltage deviation value is at -25 ℃, while the minimum output voltage ripple is at 100 ℃. Also, for the boost mode, the output voltage ripple improvement percentages are 36.38%, 30%, 23.79%, 19.22%, and 10%, while the output voltage deviation improvement percentages are 92.83%, 90%, 86.86%, 78.70%, and 25.37%, respectively. Figure 6 shows the percentage improvement in boost mode for output-voltage ripple and voltage deviation.

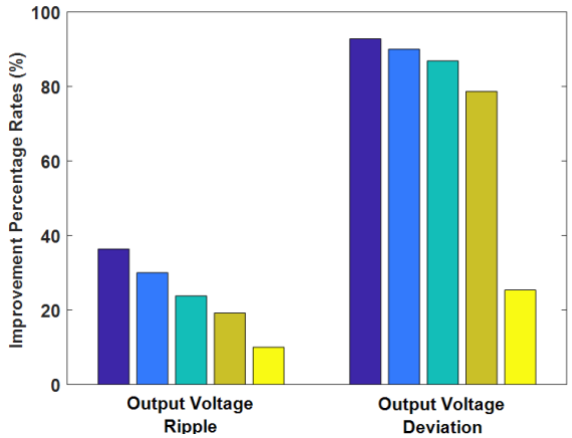

Fig. 6 – The percentage improvement rates of boost mode in terms of output voltage ripple and voltage deviation.

Similarly, Table 6 summarizes the output-voltage ripple and deviation results in buck mode for various temperature-uncertainty values.

Table 6

Output voltage ripple and deviation results in buck mode for various temperature uncertainty values

Temperature	Output Voltage Ripple	Output Voltage Deviation
-25 ℃	0.291 V	-0.127 V
0 ℃	0.243 V	-0.146 V
25 ℃	0.208 V	-0.159 V
50 ℃	0.181 V	-0.17 V
75 ℃	0.159 V	-0.178 V
100 ℃	0.14 V	-0.186 V

As shown in Table 6, the minimum output-voltage deviation occurs at -25℃, whereas the lowest output-voltage ripple is observed at 100℃. Additionally, under buck mode, the output-voltage ripple shows improvement percentages of 51.89%, 42.38%, 32.69%, 22.65%, and 11.94%, respectively, while the output-voltage deviation improves by 31.72%, 21.5%, 14.51%, 8.6%, and 4.3%, respectively. Fig. 7 illustrates the percentage improvement in buck mode for output voltage ripple and voltage deviation.

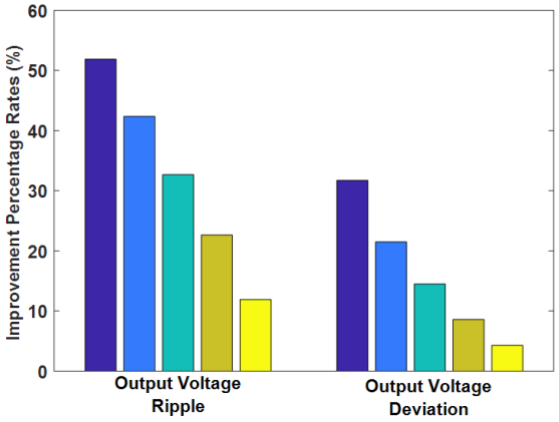

Fig. 7 – The percentage improvement rates of buck mode with respect to output voltage ripple and voltage deviation.

4.2 COMPONENT MANUFACTURING UNCERTAINTY MODEL 1

$L_1, R_{L1}, C_1, C_2, r_{C1}, r_{C2}$ varied within 20% tolerance limits, while R_0 fixed nominal value. The operating temperature values for both L_1, R_{L1}, C_1, C_2, r_{C1}, r_{C2}, R_0 and AON2392/MOSFET model are set to 25 ℃ in this scenario. Figure 8 illustrates the impact of $L_1, R_{L1}, C_1, C_2, r_{C1}, r_{C2}$ tolerance limits on the BDC, with the duty cycle fixed at $D = 0.89$ for boost mode and $D = 0.12$ for buck mode using a 50-iteration Monte Carlo simulation.

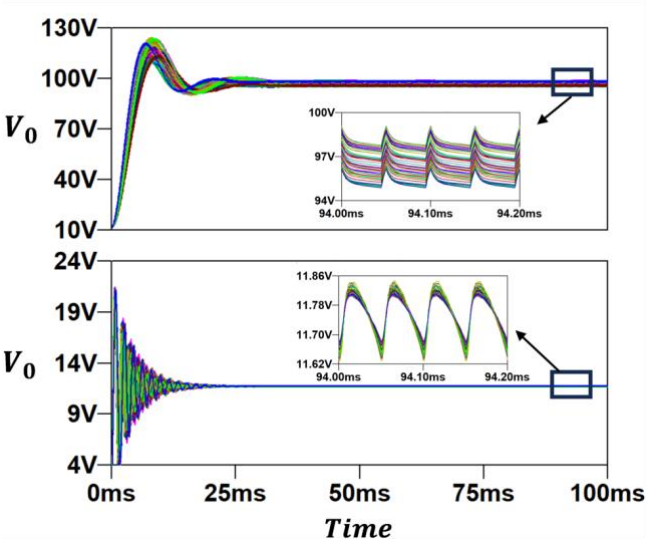

Fig. 8 – Impact of $L_1, R_{L1}, C_1, C_2, r_{C1}, r_{C2}$ tolerance limits on the BDC within boost and buck modes.

The output voltage ripple and deviation results obtained from $L_1, R_{L1}, C_1, C_2, r_{C1}, r_{C2}$ tolerance limits with boost and buck modes are presented in Table 7.

Table 7

Output voltage ripple and deviation results obtained from $L_1, R_{L1}, C_1, C_2, r_{C1}, r_{C2}$ tolerance limits with boost and buck modes.

Boost/Buck Modes	Output Voltage Ripple	Output Voltage Deviation
Boost Mode	1.309 V	1.085 V
Buck Mode	0.217 V	-0.155 V

4.3 COMPONENT MANUFACTURING UNCERTAINTY MODEL 2

The value of R_0 varied within the 5% tolerance limit, while $L_1, R_{L1}, C_1, C_2, r_{C1}, r_{C2}$ was fixed at the nominal value. The operating temperature for $L_1, R_{L1}, C_1, C_2, r_{C1}, r_{C2}, R_0$ and the

AON2392/MOSFET model was set at 25℃ in this scenario. Figure 9 demonstrates how variations in R_0 within its tolerance limit affect the BDC, as determined by a Monte Carlo simulation with 50 iterations. The duty cycle was held constant at $D = 0.89$ for boost mode and $D = 0.12$ for buck mode.

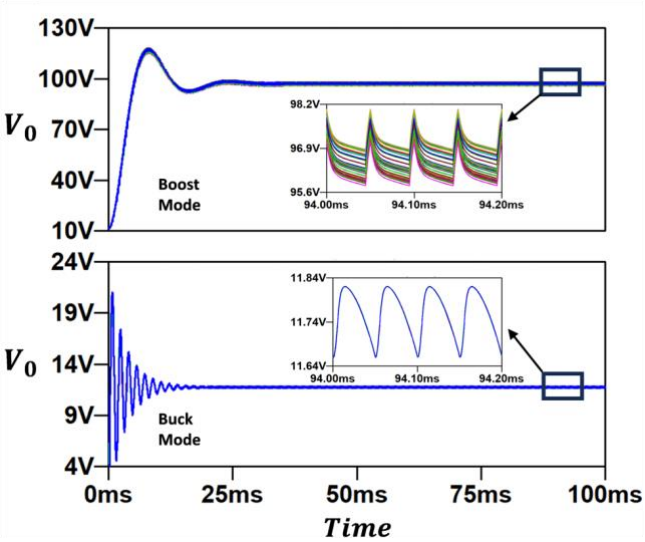

Fig. 9 – R_0 effect of tolerance limits on the BDC within boost and buck modes.

Table 8 presents the output voltage ripple and deviation results for R_0 tolerance limit in both boost and buck modes.

Table 8

Output voltage ripple and deviation results resulting from R_0 tolerance limit in both boost and buck modes.

Boost/Buck Modes	Output Voltage Ripple	Output Voltage Deviation
Boost Mode	1.197 V	0.064 V
Buck Mode	0.1605 V	0.1794 V

From the simulation results obtained in Fig. 5-9, the following observations can be made.

- As observed in Fig. 5-7. While the percentage improvement values for output voltage deviation are high in boost mode, the percentage improvement values for output voltage ripple are high in buck mode.
- As observed in Fig. 8, for buck mode, both the output voltage deviation and output voltage ripple values are lower compared to boost mode.
- As observed in Fig. 9, while the output voltage deviation value is low for boost mode, the output voltage ripple value is low for buck mode. The lower tolerance limit of R_0 compared to other scenarios has reduced the output voltage ripple in buck mode. This indicates lower sensitivity to R_0.
- As observed in Tables 7-8, for both boost and buck modes, the relatively lower tolerance limit of the R_o compared to $L_1, R_{L1}, C_1, C_2, r_{C1}, r_{C2}$ resulted in a reduction in output voltage ripple, while leading to an increase in output voltage deviation.

5. CONCLUSIONS

This paper presented a Monte Carlo-based uncertainty analysis of a non-ideal bidirectional DC-DC converter supplying a resistive DC load. Component tolerances, parasitic resistances, and temperature variations were simultaneously randomized to investigate their combined influence on DC bus voltage regulation performance.

The obtained results confirmed that the converter maintains stable operation in both boost and buck modes under realistic manufacturing and operational uncertainties. Although parameter variations affect output voltage ripple and voltage deviation, the DC bus voltage remains within acceptable operating limits, demonstrating the robustness of the converter under uncertain conditions.

In addition, the analysis revealed that parasitic effects and temperature-dependent parameter variations significantly influence the converter performance. Therefore, uncertainty-oriented analysis should be considered an essential part of practical power converter design and reliability evaluation.

Future studies will focus on nonlinear dynamic load conditions, battery and energy storage integrated systems, experimental verification, and advanced adaptive or fault-tolerant control strategies to further improve converter robustness under severe uncertainty scenarios.

CREDIT AUTHORSHIP CONTRIBUTION STATEMENT

AHMET GANI conceived the research idea and defined the study's scope. He contributed to modeling the bidirectional DC-DC converter, supported the interpretation of the results, and assisted with the technical validation of the analysis.

SEZAI ALPER TEKIN developed the Monte Carlo-based uncertainty analysis framework, performed the simulations, and analyzed the results.

Both authors contributed to the writing, critical revision, and final approval of the manuscript.

Received on 10 February 2026

REFERENCES

1. M.D. Drid, S. Hamdani, A. Nait-Seghir, L. Chrifi-Alaoui, D. Mehdi, A. Kouzou, S. Drid, *Fault-tolerant, capable, and scalable two-time-scale boost converter meant for residential areas*, Rev. Roum. Sci. Techn. – Électrotechn. et Énerg., **70**, *3*, pp. 373–378 (2025).
2. J. Marimuthu, E.R.S. Nadar, *Maximum ripple eliminating multi-level bidirectional DC-DC converter via optimized deep learning network*, Rev. Roum. Sci. Techn. – Électrotechn. et Énerg., **71**, *1*, pp. 127–132 (2026).
3. A. Ethirajan, R. Ramabadran, *Power loss analysis and control of a bidirectional high-gain converter for EV charging using PV array*, Rev. Roum. Sci. Techn. – Électrotechn. et Énerg., **71**, *1*, pp. 33–38 (2026).
4. T.I. Voicila, G.C. Seritan, B.A. Enache, *Analysis of bidirectional DC-DC power converters for screening systems of retired batteries*, Rev. Roum. Sci. Techn. – Électrotechn. et Énerg., **69**, *3*, pp. 311–316 (2024).
5. D. Ertekin, M. Ozden, *Adaptive neuro fuzzy control of a high gain bidirectional power converter for photovoltaic-hydrogen renewable electric vehicles with enhanced lifespan and reliability*, AEU-International Journal of Electronics and Communications, **156**, pp. 1–10 (2026).
6. A. Davoudi, J. Jatskevich, *Realization of parasitics in state-space average-value modeling of PWM DC-DC converters*, IEEE Transactions on Power Electronics, **21**, *4*, pp. 1142–1147 (2006).
7. J. Gajda, T. Sidor, *Using Monte Carlo analysis for practical investigation of sensitivity of electronic converters with respect to component tolerances*, Electrical and Electronic Engineering, **2**, *5*, pp. 297–302 (2012).
8. S. Peyghami, F. Blaabjerg, P. Palensky, *Incorporating power electronic converters' reliability into modern power system reliability analysis*, IEEE Journal of Emerging and Selected Topics in Power Electronics, **9**, *2*, pp. 1668–1681 (2021).
9. J. Zhang, J.S. Lai, W. Yu, *Bidirectional DC-DC converter modeling and unified controller with digital implementation*, Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition, Austin, TX, pp. 1–10 (2008).
10. K. Suresh, R. Arulmozhiyal, *Design and implementation of bi-directional DC-DC converter for wind energy system*, Circuits and Systems, **7**, *11*, pp. 3705–3722 (2016).
11. D. Hart, *Power electronics*, 1st ed., McGraw-Hill Publications, pp. 1–

500 (2010).
12. Z. Mohellebi, N. Oudni, O. Mezine, *Effect of defect geometry in a composite on reliability*, Rev. Roum. Sci. Techn. – Électrotechn. et Énerg., **70**, *4*, pp. 477–482 (2025).
13. S.A. Tekin, A. Gani, *Design and stochastic performance analysis of non-ideal ultra-lift Luo converter: A Monte Carlo approach*, Journal of Electrical Engineering Slovak University of Technology in Bratislava, **77**, *1*, pp. 89–96 (2026).
14. T. Micu, D. Micu, *The Monte Carlo method in non-homogeneous media for evaluating the risk of explosion in tanks*, Rev. Roum. Sci. Techn. – Électrotechn. et Énerg., **70**, *2*, pp. 165–168 (2025).