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A SINGLE SWITCH NON-ISOLATED QUADRATIC HIGH GAIN CONFIGURATION FOR RENEWABLE ENERGY APPLICATIONS

JAYANTHI KATHIRESAN[1], NARTHANA SIVAPERUMAL[2], GNANAVADIVEL JOTHIMANI[1], MURALADHARAN SRINIVASAN[1]

Keywords: Active switched inductor; Voltage doubler; DC-DC converter; Quadratic high gain; Continuous conduction mode.

This article presents a quadratic high-gain (QHG) transformerless DC-DC converter that integrates an active switched inductor (ASL) and a voltage doubler (VD) to achieve high voltage gain across a wide duty cycle range using a single switch. The design ensures steady input current, uses a simple continuous conduction mode (CCM), and lowers voltage stress on components—enabling the use of efficient low-resistance, low-voltage MOSFETs. By eliminating transformers and coupled inductors, it reduces size, weight, and leakage issues. Steady-state mathematical and efficiency analyses support the operating principles. A comparative study highlights its advantages, and a 100 W prototype is validated using a Simulink model.

1. INTRODUCTION

In recent decades, high step-up DC–DC conversion has garnered significant interest with the development of semiconductor switches, and their usage is facing the consistent growth in renewable energy (RE) applications. For maximum energy extraction from RE sources like solar photovoltaic (PV) modules and fuel cells, continuous source current DC structures are widely employed to effectively optimise the energy conversion [1,2]. Typically, it is essential to raise the low voltage levels trapped from the solar, batteries, wind, and fuel cells to a high bus voltage at high efficiency and at the cheapest cost. Particularly, the major attributes of lower semiconductor stress, simplicity, and resilience of the related topologies are frequently cited as the primary factors in DC–DC conversion. The most popular architecture for this purpose is the typical non-isolated boost converter, even though the conversion efficiency is restricted at greater values of duty cycles [3,4]. However, the typical boost converter is not suitable for such applications since it requires excessive duty cycles and has high power losses. New power converter topologies are continuously being introduced in recent literature reports, intending to meet the desire for such factors. These topologies employ a limited amount of active and passive components along with a range of voltage-boosting strategies. Many novel topologies and structures are possible via distinct self-lifting cells with extra components, are challenging to understand [5,6].

Regrettably, a lot of diodes and capacitors could be required in applications with very high gain, which raises the cost and reduces efficiency. Furthermore, these structures could face issues with electromagnetic interference and diode reverse recovery, necessitating the adoption of extra snubbers and coupled inductors (CI) that incur minimal losses [7,8]. On the other hand, Imanlou, A. et al [9] claimed a novel high-gain topology with a combination of active switched inductor (ASL) and switched capacitor (SC) networks, and possesses the capacity to attain a steady gain through a variety of duty ratio configurations.

However, the design and control are a difficult task due to the simultaneous control of both duty cycles. Additionally, in CI-based converters, the switch notices a large shoot up in the voltage due to leakage inductance, which could further cause large strain in the power devices and decrease the efficiency. In this regard, the stress on the diodes might be diluted by increasing the time of power delivery to the output by the standard design of Z-source (ZS) configuration [10]. However, this topology application is further restricted by the intermittent source current and the lack of a common ground between the input and output sides. Henceforth, in order to address these problems, several other alternative ZS architectures are now offered in the literature, with a common ground and minimal strain on the converter components [11–13]. On the other hand, the research in [14,15] introduces a novel kind of quasi-impedance and resonant-based DC-DC converter to obtain a huge boost ratio, with lowered stress on the switching device compared to the traditional quasi structures.

Despite the merits noticed in the aforementioned reports, few articles have shown interest in employing quadratic-type boost and buck-boost configurations to further augment the gain even at a lesser duty ratio [16-18]. Apart from traditional ones, few studies have documented Sepic-based quadratic converters, which are acknowledged for the unique features of a high boost factor to get around existing restrictions [19]. Moreover, Sepic topology combined with the ASL and multiplier nets with low voltage stress and current ripple has been investigated in [20,21]. Regardless of the notable improvements in the performance metrics of the abovementioned converters, the study in [22–23] incorporates CI to ameliorate their voltage gain. On the contrary, the envisaged structures introduced in [24-26] belong to another set of high-gain converters, which includes the amalgamation of lifting cells to notice the drastic improvement in the efficiency and voltage amplification. Apart from the aforementioned converters, Ahmed Farouk Kasse et al. [27] claimed the integration of a multilevel converter with the low-voltage DC link that ensures stability in the PV system. This paper involves the design of a step-up architecture with the undeniable merits of (1) ceaseless input current, (2) high voltage gain, and (3) lesser burden on the switch, which is suitable for employment in renewable energy (RE) applications.

The organisation of the study is stated as follows: The theoretical analysis of the power circuit configuration has been contemplated in Section 2, whereas Section 3 depicts the computation of electric stress. The investigation on loss and efficiency of the converter is devised in Section 4, and the converter's practical results are discussed in Section 5.

[1]Department of Electrical and Electronics Engineering, Mepco Schlenk Engineering College, Sivakasi, Tamil Nadu, India.
[2]Department of Electrical and Electronics Engineering, Ramco Institute of Technology, Rajapalayam, Tamil Nadu, India.
E-mail:kjayanthi@mepcoeng.ac.in, gvadivel@mepcoeng.ac.in, smurali@mepcoeng.ac.in, narthana@ritrjpm.ac.in

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Section 6 outlines the comparative performance, followed by the conclusion that is presented in Section 7.

2. TOPOLOGICALCIRCUIT ANALYSIS

The devised quadratic high-gain (QHG) topological circuitry is shown in Figure 1. By incorporating ASL and voltage doubler (VD) cells in the quadratic boost converter, the gain is drastically improved. The QHG structure is constructed by using a single switch SW operating at a duty ratio (d), three inductors (L_1 to L_3), boosting capacitors (C_1 to C_4), diodes (D_1 to D_7), and a filter capacitor (C_5). The converter's operating states are identified using the charging and discharging states of the passive elements. Figure 2 presents the switching transition of voltage and current over the passive elements. The associated equivalent current paths for continuous conduction mode (CCM) are represented in Fig. 3.

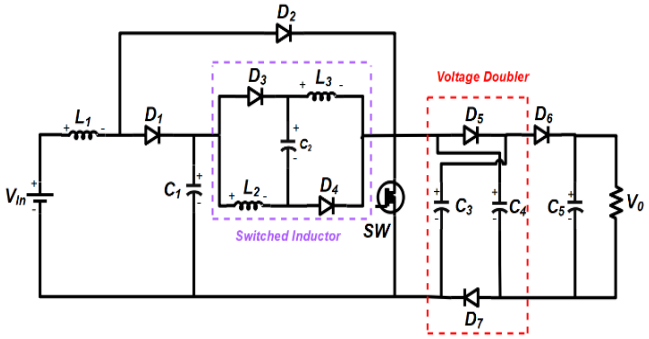


Fig. 1 – Topological power circuit.

Mode 1: When operating in first mode, SW goes into conducting state and energy gets accumulated in L_1, L_2, and L_3.This makes D_2, D_3, D_4 and$D_6$to be in conduction and D_1, D_5, and D_7 in blocked condition. Through D_3 and D_4, C_1 releases its energy and charges C_2. At the same time, C_3 and C_4 discharge via D_6, simultaneously charging C_5 to supply the necessary power to the load. As seen in the ON state diagram in Fig. 3a, the voltage that flows through the inductors may be determined using Kirchhoff's Voltage Law (KVL). The following are the mathematical expressions of voltage across inductors (V_{L1}, V_{L2}, V_{L3}) and capacitors (V_{C1}, V_{C2}, V_{C3}, V_{C4}& V_{C5}).

$$V_{in} - V_{L1} = 0, \quad (1)$$

$$V_{C1} - V_{L2} = 0, \quad (2)$$

$$V_{C1} - V_{L3} = 0, \quad (3)$$

$$V_{C1} - V_{C2} = 0, \quad (4)$$

$$V_{C4} + V_{C3} - V_{C5} = 0, \quad (5)$$

where V_{in} signifies the input voltage, and V_{C5} equals the load voltage V_0.

Mode 2: During this period, D_1, D_5, and D_7 are active, while D_2, D_3, D_4, and D_6 are under reverse bias conditions, and SW enters the OFF condition. In this phase, the energy accumulated in C_2, L_2, and L_3 is passed on to charge C_3 and C_4 via D_5 and D_7. The charging of C_1 occurs through V_{in} and L_1. The load gains the power from C_5. The associated equations are expressed in eq. (6)-(8):

$$V_{in} - V_{L1} - V_{C1} = 0, \quad (6)$$

$$V_{in} - V_{L1} - V_{L1} - V_{L3} + V_{C2} - V_{C3} = 0, \quad (7)$$

$$V_{C5} = V_0. \quad (8)$$

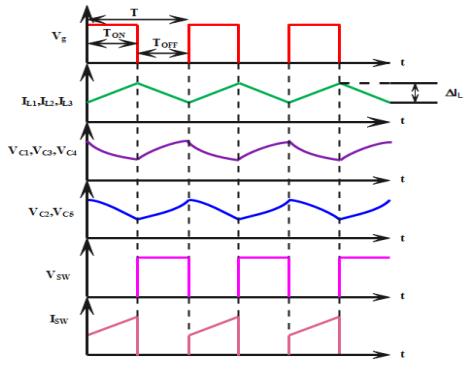


Fig. 2 – Key analytical waveforms of converter elements.

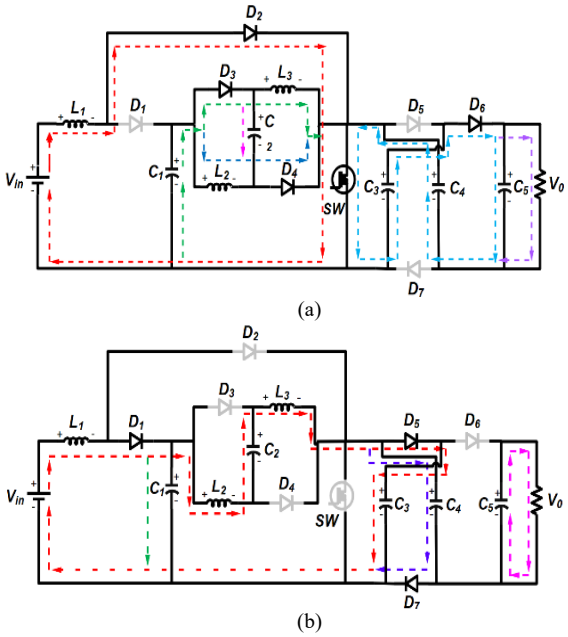


Fig. 3 – Operating equivalent circuits; a) Mode-1; b) Mode-2.

Adopting the fundamental principle of voltage balance to the above-mentioned equations, the voltage gain (G) can be determined as follows:

$$V_{C1} = \frac{V_{in}}{1-d}, \quad (9)$$

$$V_{L1} = \frac{V_{C1}+V_{C2}-V_{C4}}{2}, \quad (10)$$

$$V_{C1} = \frac{V_0(1-d)}{4}, \quad (11)$$

$$G = \frac{4}{(1-d)^2}. \quad (12)$$

3. DESIGN AND STRESS COMPUTATION

3.1 CHOICE OF INDUCTORS

The presented circuit's inductor design is based on the parameters of d, switching frequency (f_S), and ripple current. The generic design for the inductors is acquired from eq. (13) as follows,

$$V_L = L\frac{di}{dt} = V_{in}, \quad ,(13)$$

where di/dt is the change in inductor current, V_L and ΔI_{L1} denote the inductor's voltage and ripples as shown in,

$$\Delta I_{L1} = \frac{V_{in}dT}{L_1}, \quad (14)$$

$$L_1 = \frac{Rd(1-d)^4}{4f_s}, \quad (15)$$

$$L_2 = L_3 = \frac{Rd(1-d)^2}{2f_s}. \quad (16)$$

3.2 CHOICE OF CAPACITORS

The selection of a capacitor depends on similar parameters as described in the previous sub-section, except output current (I_0) and permissible ripple voltage ($\Delta V_{C1\text{-}C5}$). The selection of capacitors is based on eq. (17)–(19).

$$C_1 = C_2 = \frac{4I_0}{(1-d)\Delta V_{C1} f_s}, \quad (17)$$

$$C_3 = C_4 = \frac{2I_0 d}{\Delta V_{C3} f_s}, \quad (18)$$

$$C_5 = \frac{(1-d)I_0}{\Delta V_{C5} f_s}. \quad (19)$$

3.3 DEVICE VOLTAGE STRESS

Equation (20) gives the burden on SW in terms of V_0 during both the operating phases.

$$V_{SW} = \frac{V_0}{2} = \frac{2V_{in}}{(1-d)^2}, \quad (20)$$

Voltage across the power diodes ($V_{D1\text{-}D7}$) is obtained and given in eqs. (21) to (23):

$$V_{D4} = V_{D5} = V_{D6} = \frac{V_0}{2} = \frac{2V_{in}}{(1-d)^2}, \quad (21)$$

$$V_{D2} = V_{D3} = \frac{V_0}{4} = \frac{V_{in}}{(1-d)^2}, \quad (22)$$

$$V_{D1} = V_{D7} = \frac{V_0}{8} = \frac{V_{in}}{2(1-d)^2}. \quad (23)$$

3.4 DEVICE CURRENT STRESS

Equations (24) and (25) provide the current expressions via the switch (I_{SW}).

$$I_{SW} = \frac{V_0(1+d)}{Rd(1-d)^2}, \quad (24)$$

$$I_{SW} = \frac{I_0(1+d)}{d(1-d)^2}. \quad (25)$$

The corresponding average current transported through the diodes is stated in Eq. (26),

$$\left.\begin{aligned} I_{D1} &= \frac{2I_0}{(1-d)}, \\ I_{D2} &= \frac{2I_0 d}{(1-d)^2}, \\ I_{D3} = I_{D4} &= \frac{I_0}{(1-d)}, \\ I_{D5} = I_{D6} &= I_{D7} = I_0. \end{aligned}\right\} \quad (26)$$

4. INVESTIGATION ON POWER LOSS AND EFFICIENCY

The losses in the circuitry can be estimated from the conduction and switching losses on each component utilised in the schematic. The diodes' average voltages are denoted by $V_{D1\text{-}D7}$, while their internal resistances are symbolised as r_{D1}, r_{D2}, r_{D3}, r_{D4}, r_{D5}, r_{D6}, and r_{D7}. Similarly, the inductors and capacitors of the presented topology also hold their own intrinsic resistances, and they are identified as r_{L1}, r_{L2}, r_{L3}, and r_{C1}, r_{C2}, r_{C3}, r_{C4}, and r_{C5}, respectively. Both types of losses are taken into consideration when calculating the switch loss, having r_{SW} as the parasitic element of SW. The total loss of each device is given as,

$$\left.\begin{aligned} P_{Loss}^T &= P_L^{SW} + P_L^D + P_L^C + P_L^L, \\ P_L^{SW} &= P_{Cond}^{SW} + P_{Sw}^{SW}, \\ P_{Cond}^{SW} &= I_{SW_{rms}}^2 \times r_{SW}, \\ I_{SW_{rms}} &= \frac{V_0(1+d)}{Rd(1-d)^2} \\ P_{sw}^{SW} &= \frac{I_{SW\_avg} \times V_{SW} \times (T_{on}+T_{off}) \times f_S}{2}. \end{aligned}\right\} \quad (27)$$

Conduction losses over diodes can be computed as shown,

$$\left.\begin{aligned} P_L^D &= \sum_{k=1}^{7} V_{fDk} I_{Dk_{avg}} + I_{Dk_{rms}}^2 r_{Dk} \\ I_{D1_{avg}} &= \frac{2V_0}{R(1-d)} \\ I_{D1\_rms} &= \frac{4V_0}{R^2(1-d)^3} \end{aligned}\right\} \quad (28)$$

Conduction losses in capacitors ($P_L{}^C$) are enunciated as,

$$\left.\begin{aligned} P_L^C &= \sum_{k=1}^{5} I_{Ck_{rms}}^2 r_{Ck} \\ I_{C1_{rms}} &= \frac{V_0(1+d)}{R^{3/2}\sqrt{(1-d)\sqrt{d}}} \\ I_{C2\_rms} = I_{C3\_rms} &= I_{C4\_rms} = \frac{V_0}{R\sqrt{d(1-d)}} \end{aligned}\right\} \quad (29)$$

Conduction losses in inductors ($P_L{}^L$) are represented as,

$$P_L^L = \sum_{k=1}^{3} I_{Lk\_rms}^2 r_{Lk}. \quad (30)$$

Finally, the efficacy (η) of the presented topology is computed from (31), which is represented as,

$$\eta = \frac{P_0}{P_0 + P_{Loss}^T}. \quad (31)$$

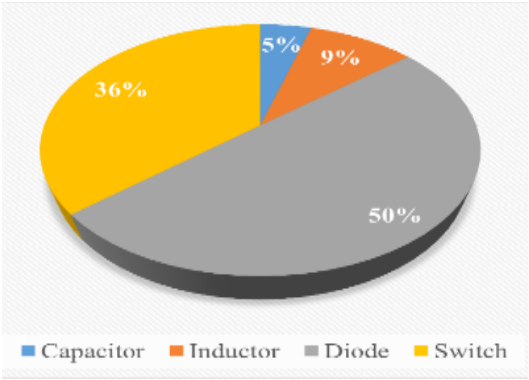


Fig. 4 – Representation of power loss on the devices.

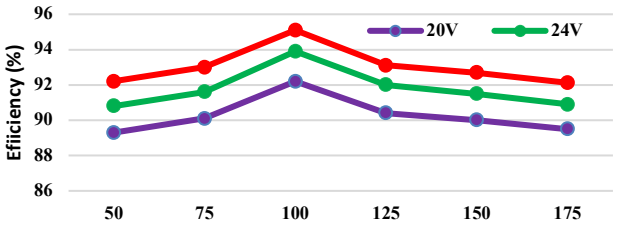


Fig. 5 – Comparative analysis of efficiency versus output power P_0.

Figure 4 depicts a pie chart of the power losses induced in the semiconductor components. This chart points out that the contribution of losses by the diodes is dominating the other converter components. It is also noteworthy that the losses due to inductors, capacitors, and power MOSFETs are low and acceptable. The comparative analysis of efficiency with dynamic changes in P_0 is plotted in Fig. 5 for distinct V_{in} of 20 V, 24 V, and 30 V.

5. EXPERIMENTAL RESULTS

This segment deals with the experimental analysis of the proposed system to validate the chosen analytical parameters. The hardware particulars are tabulated accordingly in Table 1. The working model is implemented for a 24 V input and a 240 V output at a rated power of 100 W. The MOSFET gets the gating signal from the controller board for efficient operation of the presented high-gain converter. Figure 6 picturizes the developed

hardware test bench to verify the analytical calculations and their results. The waveforms of the suggested converter are displayed in Fig. 7, operating in CCM mode at a switching frequency of 50 kHz at a nominal value of d.

Figure 7(a) shows the converter's waveforms, both at the input and output sides. The waveform shown in Fig. 7(b) portrays the current across inductor L_1 along with the gating pulse and also proves to be in accordance with the performance during its ON and OFF states. The waveforms of I_{L2} and IL3 is clearly envisaged in Fig. 7(c), whereas Fig. 7(d) presents the waveform of voltage across diode D_1 and D_7, which is measured as 40 V, indicating that the maximum burden on the switches is within the marginal values. Fig.7(e) portrays the waveform of voltage across D_2 and D_3 having their peak voltages within the acceptable limits. It is clearly noticed that the voltage across D_4, D_5, and D_6 has reached 120 V as seen in Fig. 7(f). It is also noteworthy that Fig. 7(g) agrees with the theoretical relations given in eq. (12)-(15), which depict the switch waveform blocking the voltage of 120 V during the OFF condition. All the above experimental outcomes of the devised structure, as illustrated in Fig. 7, are expected to serve as the best suitable choice for RE applications with a reasonably high peak efficiency of 95%.

Table 1

Hardware particulars

Converter Devices	Specifications
Inductor L_1, L_2, L3	400 µH, 25 A
Capacitor - C_1, C_2, C_3, C_4	100 µF, 160 V
Capacitor - C_5	150 µF, 450 V
Power MOSFET	IRFP250N, 200 V, 35 A
Power Diode	V_{RR} = 600 V, I_F =30 A (MUR3060PT)

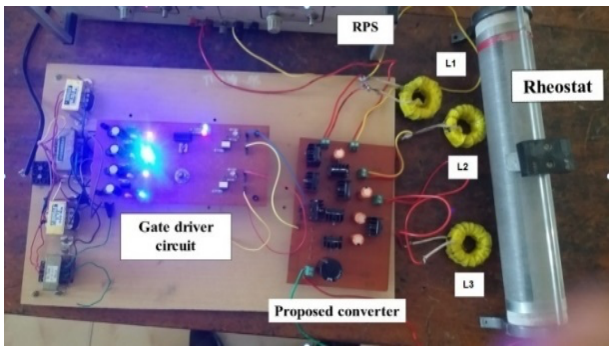


Fig. 6 – Hardware test-bench setup.

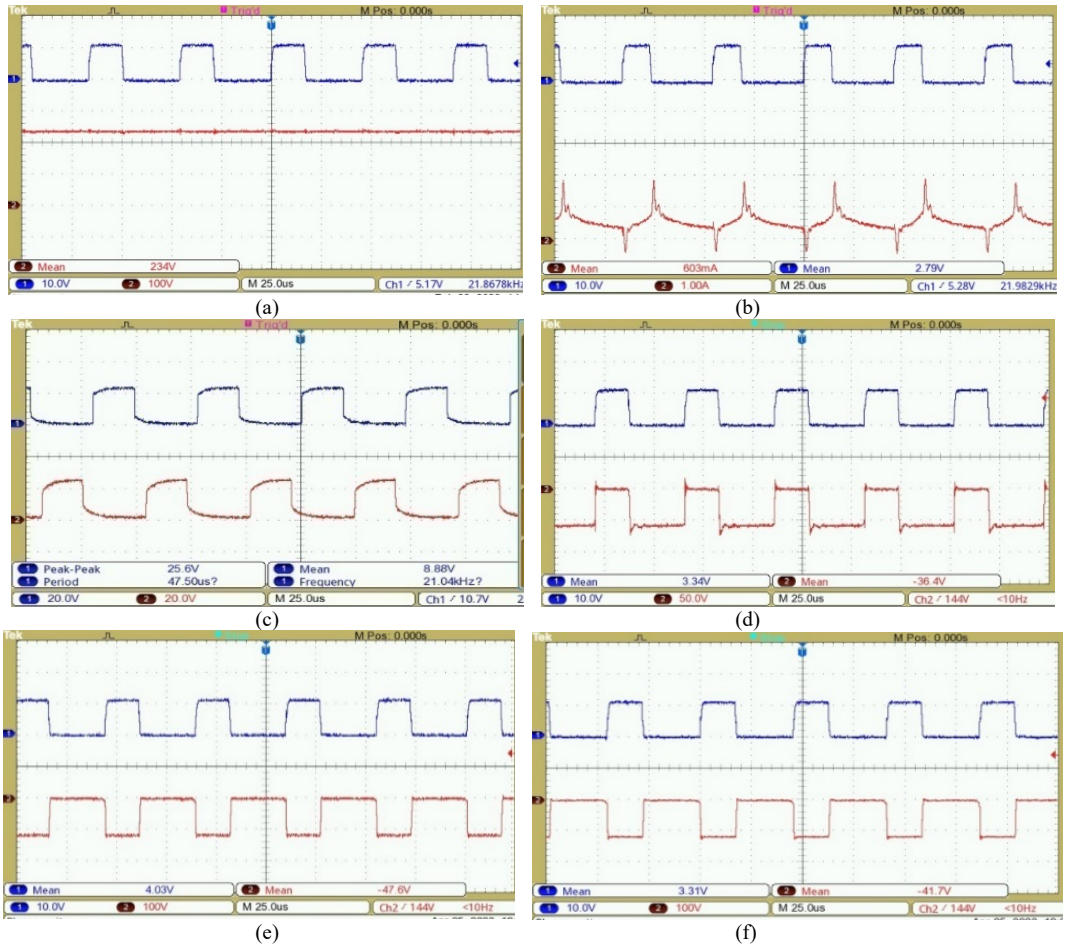


Fig. 7 – Prototype results of proposed converter; a) V_{in} and V_0; b) current through L_1; c) current through L_2 and L_3; d) voltage across D_1 and D_7; e) voltage across D_2 and D_3; f) voltage across D_4, D_5, and D_6; g) voltage across SW.

6. COMPARATIVE ANALYSIS

To highlight the performance of the QHG converter, this section conducts a thorough comparison of the proposed topology with existing high-step-up structures, as shown in Table 2. This table shows the total number of devices, voltage gain, and maximum voltage burden across switches and diodes for each structure. Figure 8 illustrates the

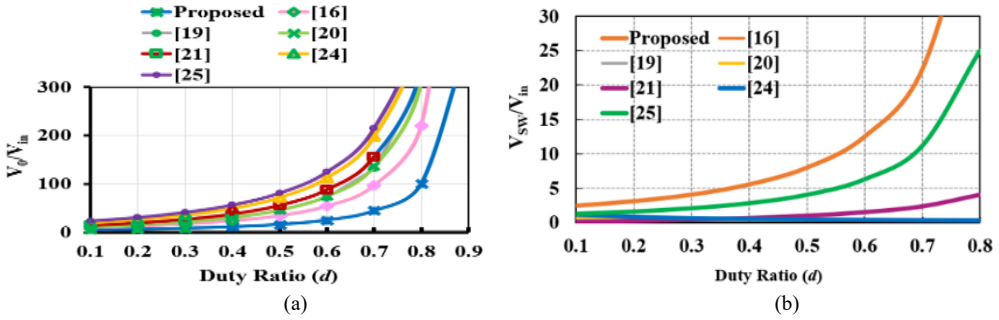
comparative performance profile of the QHG topology. The turns ratio n in Table 2 is universally defined as 2 for the sake of comparability. Figure 8(a) compares the voltage gains of various architectures, and it makes sense that the suggested converter can outperform the other five converters with the same duty cycle, except the converter in [16]. In the meantime, Fig. 8(b) provides the switch voltage stress, and it is evident that, compared to the other literature, the proposed circuit experiences less stress. According to Table 2, when device counts are considered, the topologies in [19–21] are superior to the proposed QHG configuration. However, because of the significant input current ripple, they are not appropriate for RE systems. It is also important to note that, with the same device number, the suggested converter clearly outperforms the design in [24] due to its better voltage gain, use of a single switch, and lower stresses.

Table2

Comprehensive analysis of the comparison among prevailing high-gain configurations.

Existing Topologies	Count of Elements S	D	L/CI	C	T	Voltage Gain	Maximum burden of voltage on switch	Maximum burden of voltage on diode
[16]	2	5	1/2	5	15	$\frac{2n+1+D}{(1-D)^2}$	$\frac{1+D}{2n+1+D}$	$\frac{2n}{2n+1+D}$
[19]	1	4	2/1	4	12	$\frac{n-1+nD}{(1-D)^2(n-1)}$	$\frac{n-1}{n-1+nD}$	$\frac{V_0(n-1)}{n-1+nD}$
[20]	2	1	3	2	8	$\frac{2D}{1-D}$	$\frac{V_{in}D}{1-D}$	$\frac{V_{in}}{1-D}$
[21]	2	2	3	3	10	$\frac{3nD+n-D-1}{n+D-1-nD}$	$\frac{2n-2}{3nD+n-D-1}$	$\frac{4n-2}{3nD+n-D-1}$
[24]	2	6	2	6	16	$\frac{5-D-D^2}{(1-D)^2}$	$\frac{V_{in}}{(1-D)^2}$	$\frac{V_{in}(2-D)}{(1-D)^2}$
[25]	1	8	3	5	17	$\frac{3(1+D)}{1-D}$	$\frac{V_0}{2}$	$\frac{V_0}{2}$
Proposed	1	7	3	5	16	$\frac{4}{(1-D)^2}$	$\frac{2V_{in}}{(1-D)^2}$	$\frac{2V_{in}}{(1-D)^2}$

S – Switches; D – Diodes; L/CI – Inductor/Coupled Inductor; C – Capacitor; T – Total count of elements



(a) (b)

Fig. 8 – Comparison profile of the QHG converter; (a) V_0/V_{in} for varying d; (b) $V_{SW}/V_{in}$for varying d.

7. CONCLUSIONS

This article analyses a transformerless uplifted DC-DC converter where the output voltage can be raised using the structure of ASL-VD. The recommended setup provides a straightforward design that produces the increased gain with a single power switch. The structure also offers broad conversion capability at low cost, continuous current at the input, and high efficiency. The investigation on the converter's operating modes and its steady-state analysis is accomplished. The exhaustive comparison of converter characteristics is closely examined with the other persisting topologies for better clarification. In addition, MATLAB/Simulink is used to perform the performance analysis, and a hardware configuration with a 100 W power rating at 240 V is created and tested to confirm the results. With a 95% peak efficiency, the converter finds use in solar PV applications, electric vehicles, cars, and fuel cells.

By adding control modifications, the suggested topology's potential capacity can be increased to enable bidirectional power flow for battery charging or discharging in on-board EV chargers. Additionally, to increase converter efficiency to greater power levels, soft-switching methods can be used.

CREDIT AUTHORSHIP CONTRIBUTION STATEMENT

Jayanthi Kathiresan: Main conceptual ideas, Design and Simulation
Narthana Sivaperumal: Analysis and writing of manuscript
Gnanavadivel Jothimani: Conceived the original idea and supervised the project.
Muralidharan Srinivasan: Conceived the study and oversaw overall direction and planning.

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