



GAIN ENHANCEMENT AND RIPPLE MINIMIZATION OF SPLIT SOURCE INVERTER

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Numerous DC-AC inverters have recently been created for solar systems. The split source inverter (SSI) is gaining popularity among them because of its one-stage functioning. This paper presents a modification of SSI's conventional configuration (CC) into a unidirectional DC-AC configuration for better efficiency, total harmonic distortion (THD), inductor current ripple, and capacitor voltage ripple. Different control strategies have been implemented to achieve higher gain and reduced ripple and filter requirements. The MATLAB/Simulink environment is utilized for the simulation study, and the modified topology's performance is compared with the CC-SSI. This paper proposes optimizing SSI's inductance and capacitance network parameters to enhance gain and minimize ripple using an artificial neural network model in MATLAB. The hardware prototype is built, and the simulation results are validated.

1. INTRODUCTION

Every day, there is an increasing energy demand, which needs to be supplied significantly and sustainably. Therefore, it is suggested that we opt for inexhaustible energy sources such as solar and wind energy. Photovoltaic panels are employed for trapping solar energy, which provides a DC voltage that can be boosted by a boost converter since the output from the PV panels is low and inverted into AC using an inverter [1]. This two-stage conversion requires two independently controlled power converters, *i.e.*, a DC-DC step-up converter and a DC-AC inverter. This type of conversion is quite expensive, occupies more space, and possesses lesser efficiency. Therefore, single-stage conversion is preferred where the boosting and inverting operation is incorporated into a single circuit.

Traditionally, DC to AC conversion is achieved through a voltage source inverter (VSI) or Current source inverter, depending on the requirements. The limitations of these traditional inverters include limited voltage gain (G) and high THD. To overcome this restriction, the input DC voltage is increased by inserting an impedance source network between the voltage source and the inverter circuit [2]. Different impedance source networks are available for single-stage conversions, such as Z-source, quasi Z-Source networks (qZSN), *etc.* Z-source Inverter (ZSI) uses an additional 'shoot through' switching state where the switches of the same leg would turn on for a short period, and boosting is achieved during this state. In non-shoot-through states, inversion is achieved [3]. Despite achieving boosting, the ZSI has certain drawbacks, including high voltage stress and discontinuous DC link voltage. Therefore, a quasi Z-source inverter (qZSI) is used, which has an impedance source network similar to the ZSI with slight modification [4]. The qZSI has the same modes of operation as a ZSI and provides continuous DC-link voltage for PV applications. As the number of switching states is higher in qZSI, the losses are also high [5].

Apart from ZSI and qZSI, several high-gain and multilevel inverters have been developed [6–8]. However, these topologies have a high number of passive devices, aiding in losses and reducing the system's efficiency. To overcome these disadvantages, a split-source inverter (SSI) is proposed in this work [9].

SSI consists of a traditional H-bridge structure for switches and an impedance network consisting of fewer reactive components for boosting. This inverter does not require any additional switching states like ZSI and qZSI.

The advantages of SSI are:

- Reduced number of reactive components
- Reduced voltage stress across switches
- Higher gain and reduced total harmonic distortion.

SSI has been modified to improve its performance [10]. This paper discusses modified SSI (MSSI) for managing the input and output of the inverter independently during closed-loop control [11–13]. It uses a decoupled strategy where a typical cathode arrangement is utilized to lessen the voltage spike across switches and obtain reduced parasitic inductance in the diode commutation direction instead of two distinct diodes. Doing this increases the inverter's gain and reduces its voltage and current ripple.

Along with the topological modifications, the modulation techniques used also significantly impact the performance of the inverter. Different pulse width modulation techniques (PWM) have been investigated to identify the best-suited method that yields high gain and low THD [14–16]. Further, ANN-based optimization is proposed to optimize the values obtained for the chosen PWM. The ANN-based design approach is adopted to optimize the performance parameters of the power electronic circuits using physical or electrical constraints [17,18]. Hence, an ANN-based optimization of network parameters uses a feed-forward network for the proposed inverter to obtain the optimum gain and ripple values. This paper discusses the operation of SSI in section 2, modulation schemes for SSI in section 3, simulation study in section 4, ANN-based optimization in section 5, development of hardware prototype and its results in section 6, and the paper's conclusion is given in section 7.

2. OPERATION AND ANALYSIS OF SINGLE-PHASE SSI

The single-phase SSI provides an advanced and cutting-edge single-stage conversion process. As the term suggests, the inversion and boosting procedures are completed in a single stage by splitting the DC source from the DC connection, which charges and discharges the inductor and capacitor [11].

2.1. CONVENTIONAL SSI (CSSI)

CSSI utilizes two separate diodes to link the boosting inductor to the H-Bridge. This results in a greater parasitic inductance in the diodes' commutation path.

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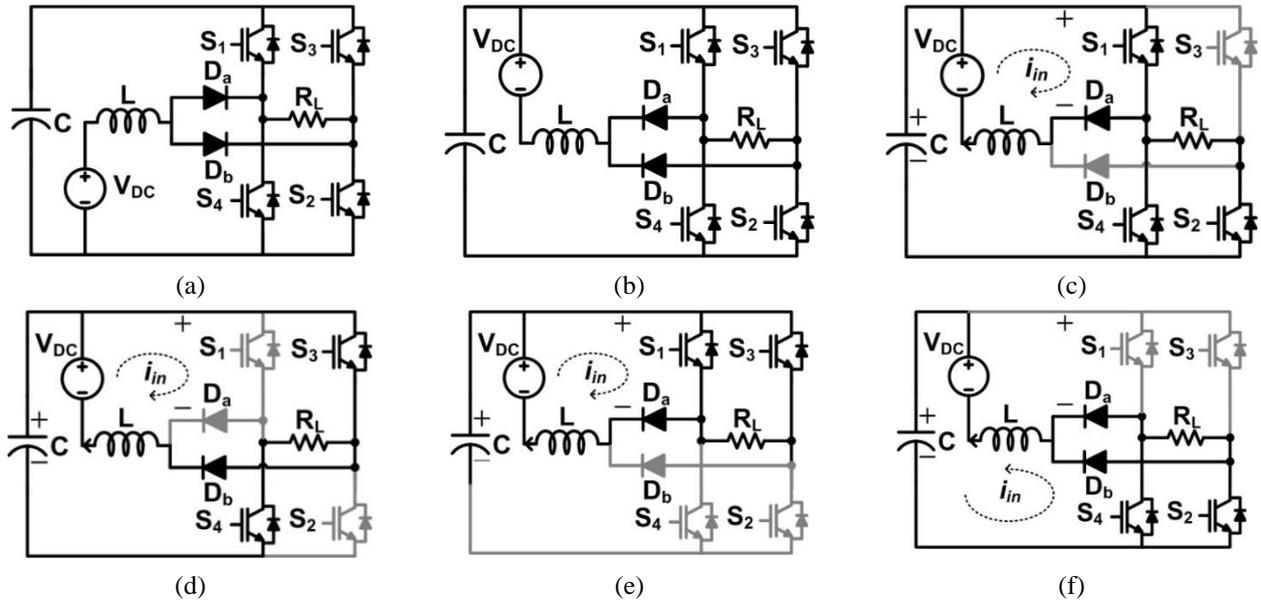


Fig. 1 – Circuit diagram; a) CSSI; b) MSSSI; and modes of operation of MSSSI; c) AS10; d) AS01; e) ZS11; f) ZS00.

As a result, voltage spikes across the switches will also be higher. Thus, the performance of SSI will be affected [13]. The topology of the single-phase CSSI which utilizes two separate diodes to link the boosting inductor to the H-Bridge is shown in Fig. 1a.

To get around all these drawbacks and improved performance, a modified configuration is needed, and that configuration is Modified SSI. 2.2.2 MODIFIED SSI (MSSSI)

MSSSI has two common-cathode dual-diode configurations to link the boosting inductor to the H-bridge. With this, parasitic inductance is minimized in the diodes' commutation path [11,13]. Also, the spikes in voltage across the switching devices in MSSSI is reduced when compared to CSSI, due to the availability of the continuous dc link voltage. As a result, the overall performance of the MSSSI has been improved, resulting in the following advantages over CSSI are high voltage gain, low THD, less current ripple in inductor (ΔI_L) and voltage ripple across capacitor (ΔV_C).

The topology of the single-phase MSSSI which utilizes two common-cathode dual-diode configurations to link the boosting inductor to the H-Bridge and the LC filter at the output is depicted in Fig. 1b.

2.2.1. Modes of operation of MSSSI

MSSSI achieves the boosting and inversion in a single stage by employing four switching states as given by Fig. 1c–f [13]. These four switching states are split into two active states (AS) and two zero states (ZS) as AS10, AS01, ZS11 and ZS00 where the on state of (S_1, S_3) and (S_2, S_4) is indicated by '1' and '0' respectively. From Fig. 1c–f, it is observed, in the first three states, inductor (L) is charging, and in the final state, it is discharging.

The conduction of switch pairs (S_1, S_4) and (S_2, S_3) is considered an AS. The conduction of the two upper or lower switches (i.e., the Switch pairs (S_1, S_3) and (S_2, S_4)) is considered as the ZS. L will charge during two AS and one ZS. Therefore, when one or both of the upper leg switches is on, L charges. During the other ZS (i.e., two lower switches are in conduction) L will discharge and capacitor (C) charges.

2.2.2. Design of SSI

The design equations of network elements of L and C and the voltage gain (G) value of the inverter is [11].

$$L = M \times \frac{(1-M) \times I_o}{(6 \times \pi^3 \times f_r^2 \times C \times \Delta I_L)} + \frac{(M \times V_{in})}{(f_s \times \Delta I_L)}, \quad (1)$$

$$C = \frac{((1-M) I_{in})}{(f_s \times \Delta V_{inv})} + \frac{(2 \times M \times I_o)}{(3 \times \pi^2 \times f_r \times \Delta V_{inv})}, \quad (2)$$

$$G = \frac{M}{1-M}, \quad (3)$$

where M is the modulation index, f_s is the switching frequency, f_r is the reference sine wave frequency, I_{in} is the input current, V_{in} is the input voltage, I_o is the output current and ΔV_{inv} is the DC-link voltage.

3. MODULATION SCHEMES FOR SSI

PWMTs are used mainly to assess the performance of the inverter as it controls the output voltage and influences the harmonic content [14–16]. These techniques are mainly used to control voltage within the inverter itself. As there are no additional switching states, a modulation technique used for traditional VSI can also be applied to SSI. In hopes of better performance, different modulation strategies are investigated in this project. In this project three different modulation strategies have been discussed. They are:

- Sine Pulse Width Modulation Technique (SPWMT)
- Modified Sine Pulse Width Modulation Technique (MSPWMT)
- Inverted Sine Pulse Width Modulation Technique (ISPWMT).

3.1. SINE PULSE WIDTH MODULATION TECHNIQUE (SPWMT)

A triangular wave is regarded as a carrier signal in SPWMT, whereas a sine wave serves as the reference signal [13–15]. A pulse is created to activate S_2 whenever the amplitude of reference wave exceeds the carrier and is complementary for S_1 . Similarly, a pulse is created to turn on S_4 when the amplitude of the carrier wave exceeds the phase-

shifted sine wave (180°), and vice versa for S_3 . Instead of using a single sinusoidal wave, two sinusoidal waves are used as reference wave for producing a switching state to turn on upper and lower leg switches. For instance, initially S_2 and S_4 are turned on simultaneously, before turning off S_2 , S_3 is turned on enabling two switches at lower legs to conduct and this state is the ZS. Figure 2a represents the pictorial representation of the SPWMT technique. This technique is not much preferable because of the oscillating charging and discharging of L , which increases the low-frequency component on the input side.

3.2. INVERTED SINE PULSE WIDTH MODULATION TECHNIQUE (ISPWMT)

In an attempt to reduce the THD and ripple across the inductor, ISPWMT is proposed. In this modulation strategy, an inverted sine wave is used for the carrier signal, and a reference signal modified sine is used, as presented in Fig. 2b. In ISPWMT, initially, the S_1 pulse is produced by comparing the inverted sine wave and the inverted sine carrier wave, and the obtained pulse wave is inverted to produce a pulse for S_2 so that the same switches on the same leg do not get activated simultaneously. At the same time, a constant wave is compared with an inverted sine carrier for generating a pulse for S_3 , and the pulse is inverted to produce for S_4 .

After a half cycle of the reference wave, the method of producing pulses for S_1 and S_3 , S_2 and S_4 are interchanged, *i.e.*, a sine wave earlier is converted into a constant wave, and a constant wave is converted into an inverting sine wave for the next half cycle. This reduces the network's reactive components' oscillating charging and discharging duty cycle. The pulse generated with ISPWMT is depicted in Fig. 2b. During this, the duration of comparing the constant signal with the inverted sine wave is reduced, resulting in relatively less duration for the inversion process. Due to this effect, high voltage and current ripple exist across the load, leading to high filter inductance (L_f) and capacitance (C_f) requirements.

3.3. MODIFIED SINE PULSE WIDTH MODULATION TECHNIQUE (MSPWMT)

MSPWMT reduces the oscillating charging and discharging duty cycle because of combination of a constant and varying reference waves as shown in Fig. 2c [13]. In MSPWMT, the S_1 pulse is produced by comparing the inverted sine wave and the triangular carrier, and the obtained pulse wave is inverted to produce a pulse for S_2 so that the same switches on the same leg do not get activated simultaneously. At the same time, a constant wave is compared with a triangular carrier to generate a pulse for S_3 , and the inverted pulse is fed to S_4 .

After a half cycle of the reference wave, the method of producing pulses for S_1 and S_3 , S_2 and S_4 is interchanged. A sine wave earlier is converted into a constant wave, and a constant wave is converted into an inverting sine wave for the next half cycle. This reduces the network's reactive components' oscillating charging and discharging duty cycle. The figure depicts the pulse generated using MSPWMT.

This technique reduces the presence of low-frequency components on the DC side. Apart from reduced ripple, the voltage gain obtained is high, and the filter requirements are comparatively reduced. The pulse pattern for MSPWMT is shown in Fig. 2c.

4. SIMULATION STUDY OF SSI

The input parameters for the simulation of CSSI and MSSI are portrayed in Table 1.

Table 1
Parameters for conventional and modified SSI

Parameters	Values
M	0.8
Input Power (W)	20
V_{in} (V)	21.25
f_s (kHz)	10
f_r (Hz)	50
Load, $R_L(\Omega)$	150

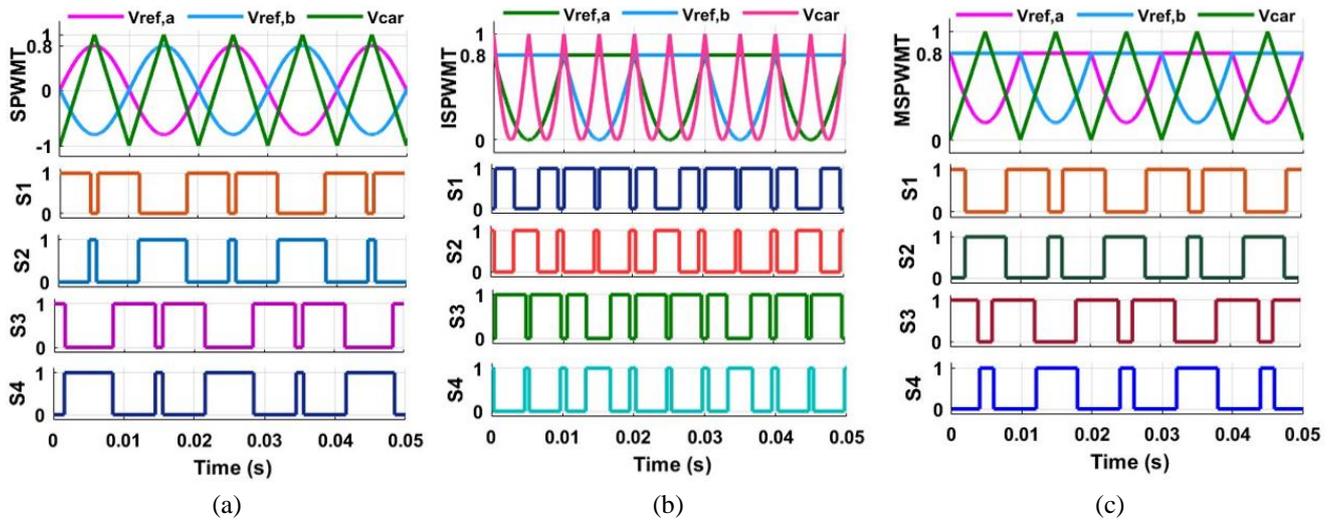


Fig. 2 – Modulation scheme: a) SPWMT; b) ISPWMT; c) MSPWMT.

4.1. SIMULATION OF CSSI AND MSSI USING MATLAB/SIMULINK

MATLAB/Simulink is used to perform the CSSI and MSSI simulation analysis. Figure 3 depicts the output voltage (V_o) and current (I_o) waveform of CSSI. According

to Fig. 3, V_o is 64.63V with a value G of 3. Figure 4 shows the V_o and I_o waveforms of MSSI using SPWMT, ISPWMT and MSPWMT. The value of V_o for SPWMT, ISPWMT and MSPWMT is 67.54 V, 76.88 V and 71.21 V with G values of 3.17, 3.61 and 3.35 respectively.

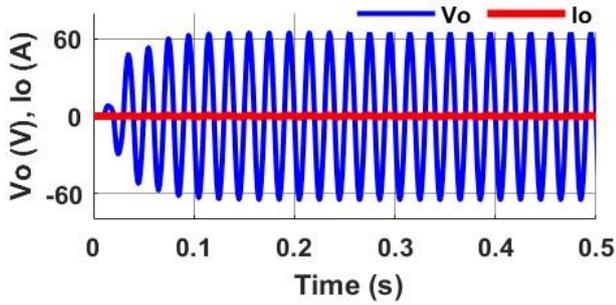


Fig. 3 – V_o and I_o waveforms of CSSI.

4.2. COMPARISON OF SSI TOPOLOGIES FOR DIFFERENT MODULATION STRATEGIES

Figures 5–8 shows the ΔV_C , ΔI_L and THD of CSSI with SPWMT and shows MSSSI with SPWMT, ISPWMT and

MSPWMT. The ΔV_C is lowest for MSPWMT and highest for ISPWMT with the values of 8V and 12V. The ΔI_L is least with a value of 0.1A for MSPWMT followed by SPWMT with 0.99A and highest for ISPWMT with 1.5A. The CSSI has a ΔI_L of 1.3A. SPWMT has the lowest THD value of 1.58% and MSPWMT has the highest value of 2.40%.

Table 2 compares conventional VSI and CSSI with SPWMT and MSSSI with SPWMT, ISPWMT, and MSPWMT. From Table 2, MSSSI has reduced THD, ΔV_C , and ΔI_L and a higher value of G than the CSSI. Among the three modulation strategies, it is observed that SPWMT and MSPWMT have low ΔI_L values, but the G of the former is lesser than the latter. Though ISPWMT provides higher gain, it has higher ΔV_C and ΔI_L . A high ripple across the L leads to reduced solar panel performance. Therefore, MSPWMT provides high G , less ΔV_C and ΔI_L , and lower L_f and C_f requirements for standard THD.

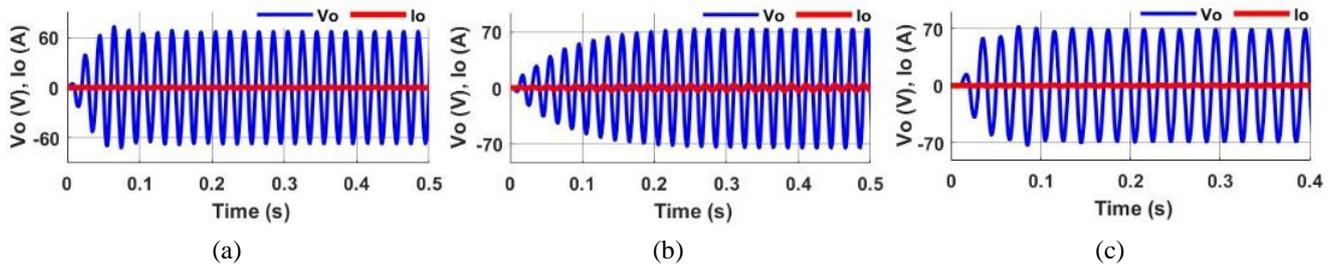


Fig. 4 – V_o and I_o waveforms of MSSSI; a) SPWMT; b) ISPWMT; c) MSPWMT.

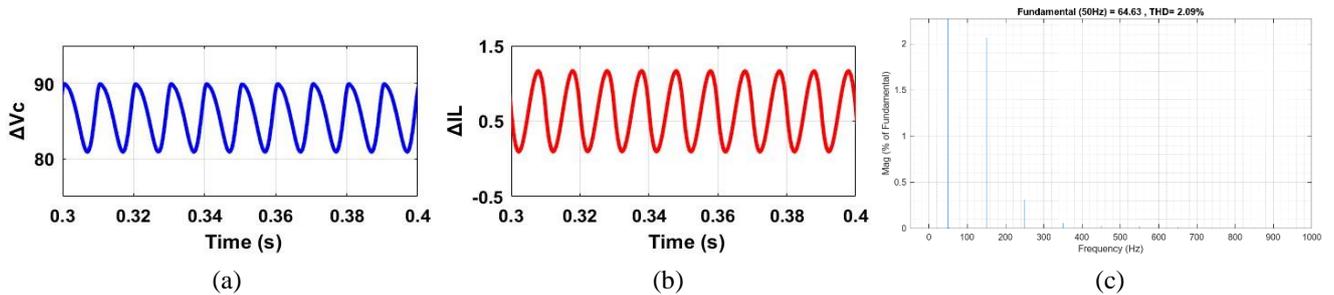


Fig. 5 – CSSI waveforms; a) ΔV_C ; b) ΔI_L ; c) THD Spectrum.

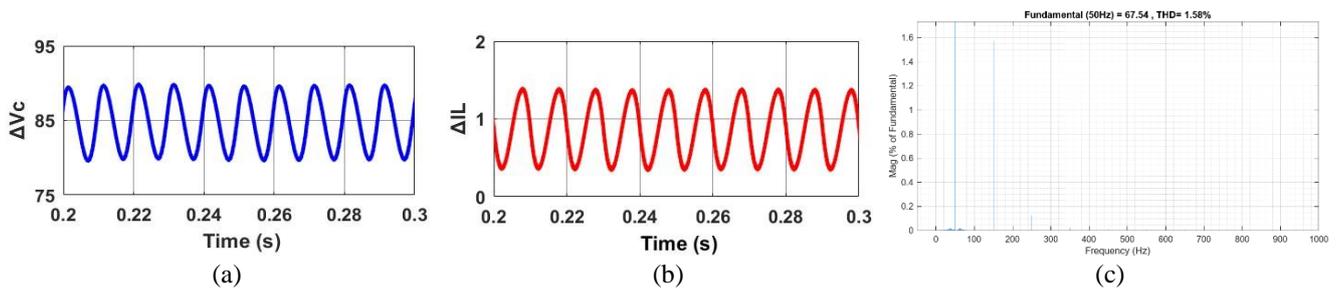


Fig. 6 – MSSSI with SPWMT waveforms; a) ΔV_C ; b) ΔI_L ; c) THD spectrum.

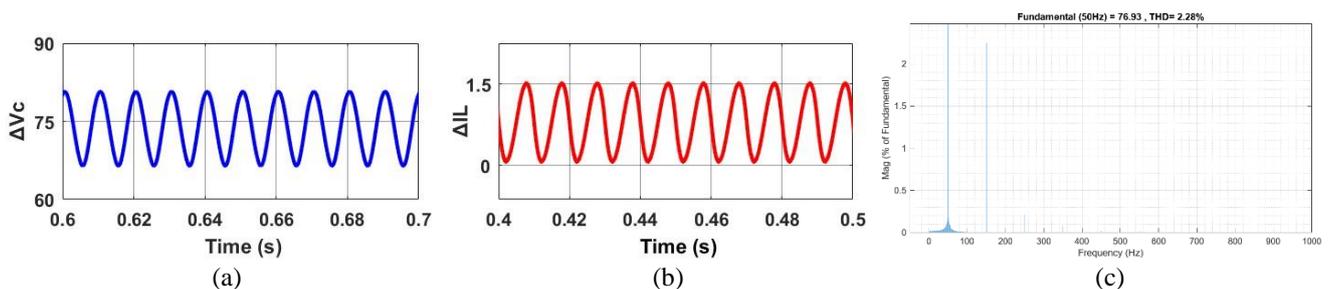


Fig. 7 – MSSSI with ISPWMT waveforms; a) ΔV_C ; b) ΔI_L ; c) THD spectrum.

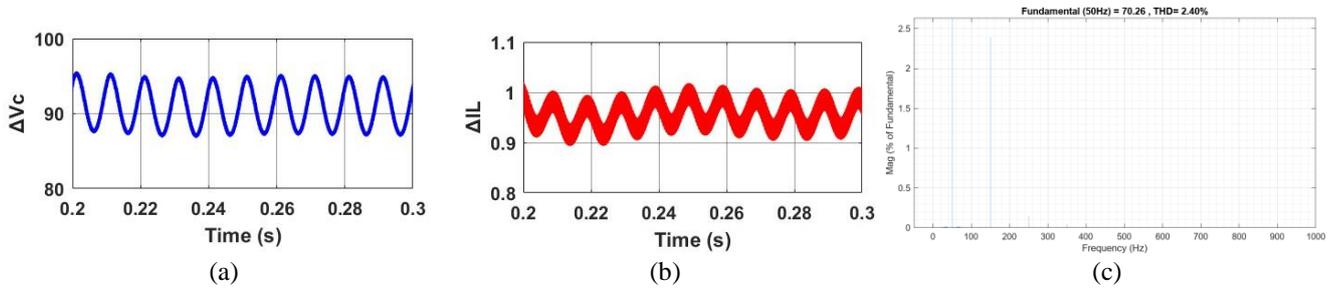


Fig. 8 – MSSI with MSPWMT waveforms; a) ΔV_C ; b) ΔI_L ; c) THD spectrum.

Table 2

Comparison of conventional and modified SSI

Parameters	Conventional SSI		MSSI		
	VSI SPWMT	CSSI SPWMT	SPWMT	ISPWMT	MSPWMT
V_o (V)	21	64.63	67.54	76.88	71.21
THD (%)	4.78	2.09	1.58	2.28	2.40
G	–	3	3.17	3.61	3.35
ΔI_L (A)	L and C	1.3	0.99	1.5	0.1
ΔV_C (V)	are absent	9	10	12	8
L_f (mH)	5	8.8	8	20	10
C_f (μ F)	440	4.5	6.02	130	20

Therefore, it can be inferred that MSSI with MSPWMT performs better among the three modulation strategies in terms of G , THD, ΔV_C and ΔI_L .

5. OPTIMIZATION OF NETWORK ELEMENTS USING ANN

An artificial neural network (ANN) is a group of artificial neurons (nodes) that closely mimic the neurons in the human brain. ANNs can “learn” to execute tasks using examples without specific programming and are used for solving optimization problems. The design of circuit parameters aims to enhance the performance of the inverter [17,18]. Therefore, the ANN is employed for optimizing the network inductance and capacitance to maximize G and minimize ΔV_C and ΔI_L .

5.1. TRAINING OF ANN

Two neural networks have been used to determine networks L and C . Each network has three inputs and one target parameter (L and C). Almost two-thirds of the data set provided to train NN is utilized to train NN, and the remaining is split equally for testing and validation. Table 3 indicates the details of the training data inputs.

A Feed-forward neural network employing an input, hidden, and output layer is developed. Only forward information flow occurs from the input node through the hidden nodes to the output nodes. This network was created and simulated using NNTOOL in MATLAB, as shown in Fig. 9. L and C requirements decrease with increasing ripple percentage. However, a higher ripple percentage leads to much higher losses. Hence, the ripple percentage inputs are less than 10% and 15% for C and L , respectively.

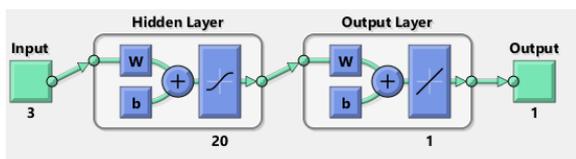


Fig. 9 – Feedforward neural network.

Thus, the optimized network element values obtained from a successfully trained NN aimed at minimizing the ripple and maximizing the gain are $L = 36$ mH and $C = 105$ μ F, whereas the previously designed values of $L = 47.9$ mH and

$C = 200$ μ F. The simulation study of the optimized parameters is studied using MATLAB/SIMULINK. V_o and I_o waveforms of optimized MSSI using MSPWM are depicted in Fig. 10.

Table 3

Details of input parameters

Parameter	Value Range	Step size
M	0.6 – 0.9	0.05
Switching frequency (kHz)	10 – 20	1
ΔV_C (%)	1 – 50	5
ΔI_L (%)	1 – 15	1

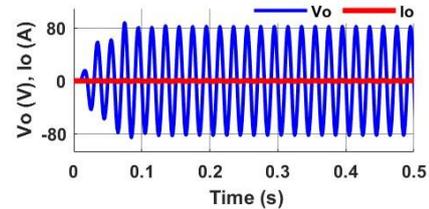


Fig. 10 – V_o and I_o waveforms of MSSI-MSPWM with optimization.

Figure 10 shows the V_o as 82 V with a G value of 3.86. Figure 11 depicts the ΔV_C , ΔI_L and FFT spectrum of MSSI after optimization. Table 4 shows that the NN optimization results in reduced values of L and C , providing a higher G value of the inverter without compromising on the ripple values, along with reduced values of THD and filter requirement.

Table 4

Comparison of Modified SSI with and without optimization

Parameter	L (mH)	C (μ F)	V_o (V)	G	ΔV_C (V)	ΔI_L (A)	THD (%)	L_f (mH)	C_f (μ F)
without optimization	47.9	200	71.21	3.35	8	0.1	2.40	10	20
with optimization	36	105	82.13	3.86	7	0.07	0.92	6.6	3

6. HARDWARE IMPLEMENTATION OF MSSI

The simulation results are validated by developing the hardware prototype for the optimized MSSI. A 20 W prototype is designed with $V_{in} = 21$ V, $L = 36$ mH, $C = 105$ μ F, $f_s = 10$ kHz, $L_f = 6.6$ mH and $C_f = 3$ μ F. The pulse for the H – bridge switches is given using the C2000 Piccolo processor. Figure 12 demonstrates the prototype model developed. The V_o and ΔV_C waveforms for MSSI is shown in Fig. 12. From Fig. 12, the V_o of MSSI is found to be 80 V and the ΔV_C is 10V. Table 5 provides the comparison of results obtained through simulation and hardware.

Table 5

Results

Result Parameters	Simulation	Hardware
V_o (V)	82	80
G	3.9	3.8
ΔV_C (V)	7	10

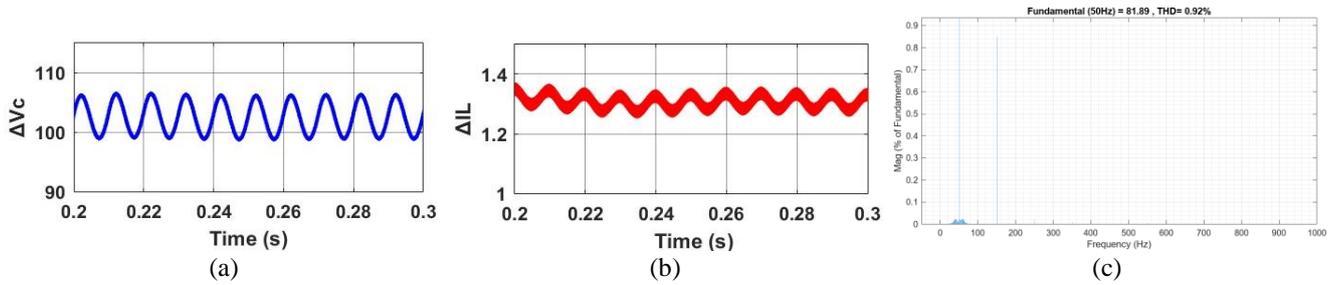


Fig. 11 –Waveforms of MSSI after optimization; a) V_C ; b) ΔI_L ; c) THD.

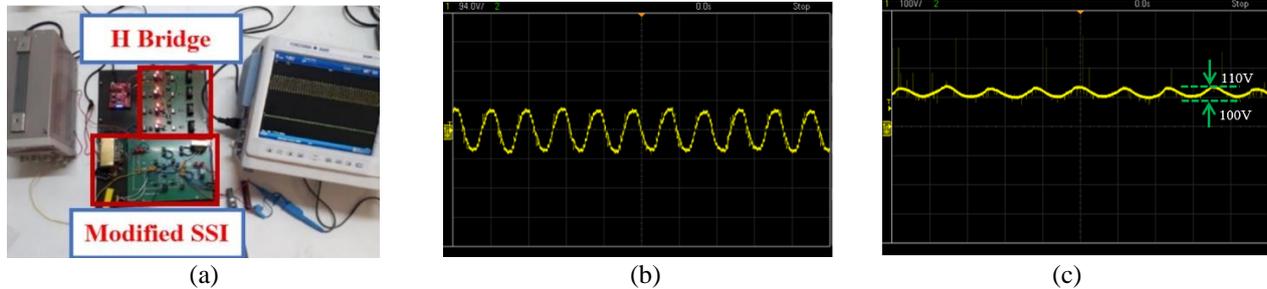


Fig. 12 – Hardware implementation of MSSI; a) prototype model; b) output voltage; c) ΔV_C .

7. CONCLUSION

This paper analyzes an MSSI for PV applications. Replacing the two separate diodes in the CSSI with the two common-cathode dual-diode configurations minimizes the diode's commutation path parasitic inductance. Three different modulation strategies have been analyzed. Among them, an MSPWMT is the best since it provides a higher voltage gain of 3.86 and reduced THD of 0.92%. The network elements L and C are optimized using the ANN model in MATLAB. The optimized network elements reduce the THD and ripple values, reducing the filter size. This enhances the compactness of the inverter with increased power density. The results demonstrate the MSSI's effectiveness for photovoltaic applications in higher G , lower THD, ΔV_C , and ΔI_L .

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CREDIT AUTHORSHIP CONTRIBUTION STATEMENT

Devi S: investigation, validation, writing - draft preparation
Seyezhai Ramalingam: methodology, resources, writing – review and editing.

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REFERENCES

- M.H. Rashid, *Power Electronics Handbook: Devices, Circuits, and Applications*, Elsevier, 3rd ed., 2011.
- F.Z. Peng, *Z-source inverter*, IEEE Trans. Ind. Appl., **39**, 2, pp. 504–510 (2003).
- M. Murali, P. Deshpande, B. Virupurwala, P. Bhavsar, *Simulation and fabrication of single phase Z-source inverter for resistive load*, U.P.B. Sci. Bull., Series C, **78**, 1 (2016).
- J. Anderson, F. Peng, *A class of quasi-Z-source inverters*, Proc. IEEE Ind. Appl. Soc. Meeting, pp. 1–7, 2008.
- L.B. Ge, Y. Abu-Rub, R.S. Balog, F.Z. Peng, H. Sun, X. Li, *An active filter method to eliminate dc-side low-frequency power for a single-phase quasi-Z-source inverter*, IEEE Trans. Ind. Electron., **8**, pp. 4838–4848 (2016).
- S. Devi, R. Seyezhai, *Impedance source inverter topologies for photovoltaic applications – a review*, International Journal of Electrical Engineering and Technology (IJEET), **12**, 11, pp. 73–85 (2021).
- M.-A. Ilie, D. Floricău, *Grid-connected photovoltaic systems with multilevel converters – modeling and analysis*, Rev. Roum. Sci. Techn.–Électrotechn. et Énerg., **68**, 1, pp. 77–83 (2023).
- D. Beriber, A. Talha, A. Kouzou, A. Guichi, F. Bouchafaa, *Multilevel inverter for grid-connected photovoltaic systems*, Rev. Roum. Sci. Techn.–Électrotechn. et Énerg., **67**, 2, pp. 105–110 (2022).
- A. Abdelhakim, P. Mattavelli, G. Spiazzi, *Three-phase split-source inverter (SSI): Analysis and modulation*, IEEE Trans. Power Electron., **31**, 11, pp. 7451–7461 (2016).
- S.S. Lee, A.S.T. Tan, D. Ishak, R. Mohd-Mokhtar, *Single-phase simplified split-source inverter (S3I) for Boost DC–AC power conversion*, IEEE Trans. Ind. Electron., **66**, 10, pp. 7643–7652 (2019).
- P. Davari, F. Blaabjerg, A. Abdelhakim, P. Mattavelli, *Performance evaluation of the single-phase split-source inverter using an alternative DC–AC configuration*, IEEE Trans. Ind. Electron., **65**, 1 (2018).
- O.G. Londhe, S.L. Shaikh, *Analysis of the single-phase split-source inverter by using different DC AC topology*, IJERT, **9** (2020).
- S.S. Harshad, S. Devi, R. Seyezhai, N. Harish, R. Bharath Vishal, V. Barath, *Design and analysis of split-source inverter for photovoltaic systems*, IoT and Analytics in Renewable Energy Systems, CRC Press, **1**, pp. 1–12 (2023).
- U. Devaraj, S. Ramalingam, D. Sambasivam, *Evaluation of modulation strategies for single-phase quasi-Z-source inverter*, J. Inst. Eng. India Ser. B, The Institute of Engineers (India), 2018.
- D. Umarani, R. Seyezhai, *Investigation of quasi Z-source cascaded multilevel inverter for PV system with maximum power point tracking*, Applied Mechanics and Materials, **622**, pp. 105–110 (2014).
- J.I.J. Kumar, C. Sajeesh, *Design and implementation of modified split source inverter with quasi sinusoidal PWM technique for stand-alone system*, International Journal of Engineering Research & Technology (IJERT), **9**, 1 (2020).
- S.E. De León-Aldaco, H. Calleja, J. Aguayo Alquicira, *Metaheuristic optimization methods applied to power converters: A review*, IEEE Trans. Power Electron., **30**, 12, pp. 6791–6803 (2015).
- X. Li, X. Zhang, F. Lin, F. Blaabjerg, *Artificial-Intelligence-Based Design for Circuit Parameters of Power Converters*, IEEE Trans. Ind. Electron., **69**, 11, pp. 11144–11155 (2022).