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A NOVEL FAULT-TOLERANT GENERALIZED SYMMETRICAL TOPOLOGY FOR RENEWABLE ENERGY AND ELECTRIC VEHICLE APPLICATIONS

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Keywords: Multilevel inverter (MLI); 13-level; 25-level; Fault-tolerant; Total harmonic distortion (THD).

Multilevel inverters are a versatile and powerful technology for applications such as motor drives, high voltage direct current transmission (HVDC), renewable energy systems, and grid-connected applications. As the demand for high-quality, clean energy and low distortion continues to grow, multilevel inverters are preferred over traditional square wave inverters. This paper proposes a generalized 13-level symmetrical topology to meet the power quality requirements. It consists of six DC sources and twelve semiconductor devices. Further, the topology has cascaded to increase the number of levels, but the cost and circuit complexity increase with the number of units. The gate pulses for switches are produced by the nearest-level modulation technique. The performance comparison of the topology with recent literature provides comprehensive information about the novelty of the configuration. The MLI performance parameters are number of switches, number of gates driving circuits, total harmonic distortion (THD), cost function per level (CCPL), total standing voltage (TSV), and efficiency (η). MATLAB/Simulink investigates the proposed topology, and further, to validate its simulation output, the hardware prototype model has been implemented in the laboratory.

1. INTRODUCTION

Multilevel inverter (MLI) is crucial for modern technologies such as renewable energy and electrical vehicle applications. Unlike traditional two-level inverters that switch between positive and negative voltage levels, MLI can produce AC waveforms with multiple voltage levels, resulting in smoother output waveforms and reduced voltage distortion. It led to various benefits, including improved efficiency, reduced electromagnetic interference, and compatibility with sensitive electronic devices [1]. The rapid advancements in renewable energy technology have led to increasingly sophisticated and efficient multilevel inverters that play a vital role in harnessing and integrating renewable energy into our electricity systems [2,3]. A renewable energy MLI is a power electronic device that converts direct current (DC) electricity from renewable energy sources, such as solar panels or wind turbines, into high-quality alternating current (AC) electricity suitable for residential, commercial, and industrial applications. It also offers other benefits, such as voltage regulation, maximum power point tracking (MPPT), monitoring and communication, grid interaction, and island protection for power systems [4]. Multilevel inverters are also used in electric vehicles (EVs). EVs need a high-power inverter to convert the DC power from the battery to the AC power required by the electric motor. It is important to note that designing and implementing multilevel inverters can be more complex than traditional inverters due to the increased number of components and control strategies involved. Even though their benefits in terms of improved output waveform quality, lower switching losses, higher efficiency, higher power density, and harmonic reduction make them attractive options for high-power and grid-connected renewable energy systems. Modular multilevel inverter is typically preferred for renewable energy and electrical vehicle applications. It comprises several smaller inverters, each producing a single voltage level [5]. The smaller inverters are then connected to make a multilevel output voltage. Modular multilevel inverters are the most complex type of multilevel inverter, but they offer the highest efficiency and lowest switching losses. Many companies manufacture multilevel inverters [6]. Some of the most well-known companies are ABB, Siemens, Schneider Electric, Yaskawa, Fuji Electric, Mitsubishi Electric, Toshiba Energy Systems & Solutions Corporation, *etc*. Based on the discussion and challenges, the paper's central focus is designing a novel symmetrical modular MLI topology with a minimum number of components. In this paper [7], the 13-level symmetrical topology is designed using 12 switches, two sources, and four capacitors. It became more complex due to voltage balancing issues. The topology proposed in [8] consists of 1 source, three capacitors, and 16 switches to generate 13-level waveforms. More switches are needed, so the cost has increased. The generalized 13-level topology has been proposed for solar energy sources, fuel cells, and battery-backed electric vehicle applications [9]. The circuit suggested [10] consists of 13 switches, three diodes, three capacitors and one source. The 13-level single-phase AC output voltage has achieved a voltage gain of six by utilizing a single DC source, 14 switches, three capacitors, and one diode in the proposed converter [11]. It employs a single source and produces a 13-level waveform by utilizing only 14 switches, two diodes, and four capacitors.

The other recently proposed 13-level individual or generalized topologies are discussed [12–16]. Based on the discussion, a novel generalized 13-level symmetrical MLI has been proposed to overcome the challenges based on recently introduced topologies. This paper subdivides into the following manner. Section 1 discusses the need for MLI and the demerits of the already proposed circuits. section-2 shows the current flow path of 13-level symmetrical topology and its switching states. Section 3 analyses the output of the generalized circuit and provides the general equations. Section 4 illustrates the simulation output of topology under different load conditions, such as R and RL loads. Section 5 implements the hardware prototype model and validates its simulation results. Section 6 concludes the work.

2. PROPOSED MLI TOPOLOGY

The topology of the proposed 13-level symmetrical MLI unit is illustrated in Fig. 1

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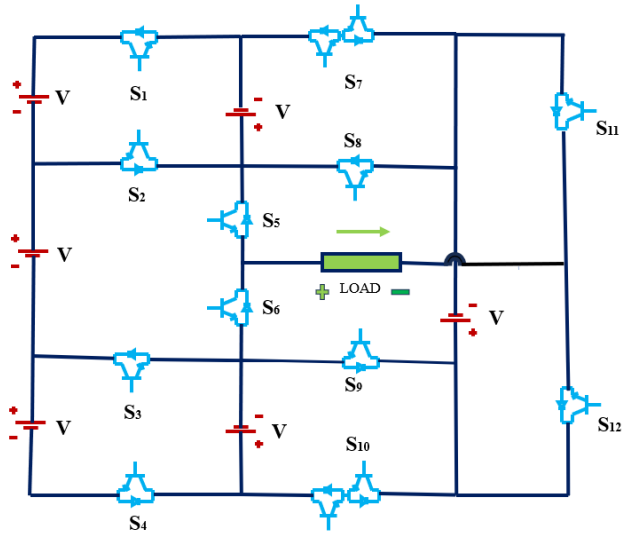


Fig. 1 – Topology circuit of proposed 13-level symmetrical MLI

This unit comprises six symmetrical DC sources (V_1=20V), 12 power semiconductor switches (S_1-S_{12}), and 12 gate driving circuits. It can generate a 13-level stepped waveform that imitates the desired sinusoidal waveform with the help of a minimum number of symmetrical DC sources and switches. The switching pulses for power devices are generated by the nearest voltage level modulation (NVL) technique. It is connected to different combinations of R and RL loads to analyze the THD value. Table 1 shows the switching states of IGBT with various combinations of on and off-gating pulses to synthesize zero, positive, and negative voltage levels across the load. The different operating modes of the proposed MLI by activating the other combination of switches are explained.

Table 1

Switching states for 13-level MLI.

Mode	Voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
1	V	0	0	0	0	1	0	1	0	0	0	1	0
2	2V	0	1	0	1	1	0	0	0	0	1	0	1
3	3V	0	1	0	1	1	0	0	0	1	0	0	1
4	4V	1	0	0	1	1	0	0	0	0	1	0	1
5	5V	1	0	0	1	1	0	0	0	1	0	0	1
6	6V	1	0	0	1	1	0	0	0	1	0	1	0
7	0	0	0	0	0	1	0	0	1	0	0	1	0
8	-V	0	0	0	0	1	0	0	1	0	0	0	1
9	-2V	1	0	1	0	0	1	1	0	0	0	1	0
10	-3V	1	0	1	0	0	1	1	0	0	0	0	1
11	-4V	1	0	0	1	0	1	1	0	0	0	1	0
12	-5V	1	0	0	1	0	1	1	0	0	0	0	1
13	-6V	1	0	0	1	0	1	0	1	0	0	0	1

Mode 01: The switches S_5, S_7, and S_{11} are powered ON to connect the one DC source through the current path (V-S_5-Load-S_{11}-S_7) for providing the V across the load

Mode 04: The current path (V-V-V-S_1-V-S_5-Load-S_{12}-S_9-V-S_4) is formed by powering the switches S_1, S_5, S_{10}, and S_4 to create the positive voltage level 4V for the load.

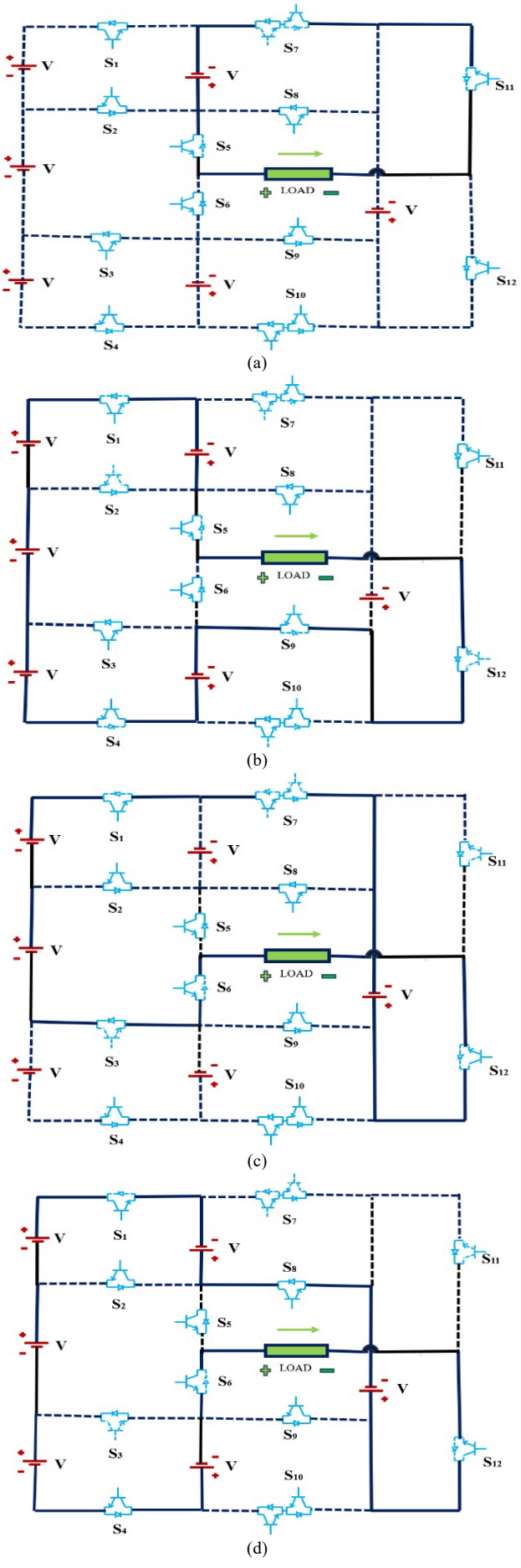


Fig. 2 – Current flow path for different modes; (a) mode 1-(V) (b) mode 4-(4V) (c) mode 10-(-3V) (d) mode 12-(-5V).

Mode 10: In this configuration, the switches S_1, S_6, S_7, and S_{12} are turned on to provide the route for load through the current path (V-V-S_1-S_7-V-S_{11}-S_{12}-Load-S_6-S_3).

Mode 12: The load voltage is -5V. Fig () shows the current flow path (V-V-V-S_1-S_7-V-S_{12}-LOAD-S_6-V-S_4), which is obtained by turning on the switches S_1, S_4, S_6, S_7, S_{12}.

3. GENERALISED MLI TOPOLOGY

Figure 3 shows the proposed fundamental 13-level symmetrical MLI unit modified as a 2-module generalized circuit. The negative load terminal of module 1 is connected to the positive load terminal of module 2. The load is connected between the positive load terminal of module 1 and the negative load terminal of module 2. It can generate 25-level step waveforms with the help of 24 switches and 12 sources.

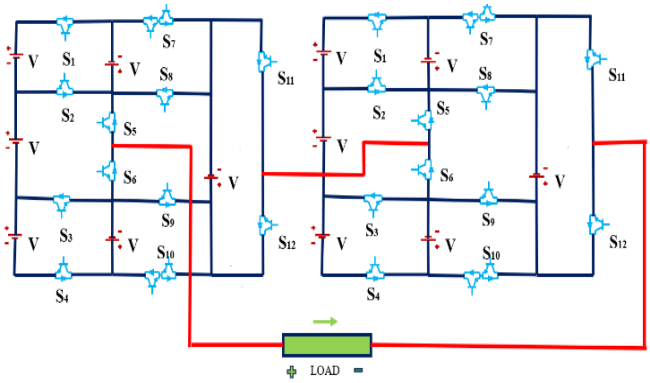


Fig. 3 – Proposed 2 module 25-level inverter.

Hence, the total harmonic distortion (THD) is diminished by increasing the levels. In the same way, a higher number of level waveforms can be produced by connecting the "n" module in series. The mathematical generalized equation can be developed for topology parameters based on the number of modules (n):

$$\text{The number of DC sources } (N_{DC}) = 6n, \quad (1)$$

$$\text{The number of unidirectional switches } (N_{SU}) = 10n, \quad (2)$$

$$\text{The number of bidirectional switches } (N_{SB}) = 2n, \quad (3)$$

$$\text{The number of gates driving circuits } (N_{GD}) = 12n, \quad (4)$$

$$\text{The number of voltage levels } (N) = 12n+1. \quad (5)$$

4. FAULT-TOLERANT CAPABILITY OF MLI

The fault-tolerant capability of the proposed 11-level topology can be verified by the failure of DC sources [17,18]. The other possible faults are failure of switches, gate driving circuits, and disconnection due to thermal heating. However, this section analyzes the fault in DC sources and its impacts on output voltage levels. The 13-level MLI output is reduced to an 11-level voltage output due to the failure of any one source. Similarly, the 9-level production is generated by the failure of two DC sources. Then, 7-level MLI is produced by the failure of three DC sources.

Further, it generates 5-level MLI by failing four DC sources, and the failure of five DC sources produces 3-level MLI. However, the harmonic distortion keeps increasing when reducing voltage levels. The switching states for 11-level MLI are shown in Table 2. MATLAB/Simulink further verifies it, displaying results in the simulation section.

Table 2

Switching states for 11-level MLI.

modes	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
1	1	0	0	0	1	0	1	0	0	0	1	0
2	1	1	0	1	1	0	0	0	0	1	0	1
3	1	1	0	1	1	0	0	0	0	1	1	0
4	1	1	0	1	1	0	0	0	1	0	1	0
5	1	0	0	1	1	0	0	0	1	0	1	0
6	1		0	0	1	0	0	1	0	0	1	0
7	1	0	0	0	1	0	0	1	0	0	0	1
8	1	0	1	0	0	1	1	0	0	0	0	1
9	1	0	1	0	0	1	0	1	0	0	0	1
10	1	0	0	1	0	1	1	0	0	0	0	1
11	1	0	0	1	0	1	0	1	0	0	0	1

5. COMPARISON ANALYSIS

The parameters of the proposed topology are compared with those of recently published literature to prove its superiority in the symmetrical MLI domain [19]. The parameters are the number of DC sources (N_{DC}), number of semiconductor devices (N_S), number of gates driving circuits (N_{GD}), component cost per level (CCpL), total standing voltage (TSV), cost function (CF) and efficiency(η). The comparison is also made in ratios such as N_{DC}/N_L, N_{GD}/N_L, and N_S/N_L to give an acceptable assessment and better understanding because different topology generates different levels. The component count per level (CCpL) is the ratio of the total number of components per level.

$$\text{CCpL} = \frac{N_S+N_{GD}+N_D+N_C+N_{DC}}{N_L}. \quad (6)$$

Then, $TSV_{p.u}$ is another crucial factor that provides a fair comparison, defined as the ratio of TSV to the number of levels. The cost function (CF) per level is used to calculate the cost of devices needed to develop the proposed topology.

$$\text{CF} = N_S + N_{GD} + N_D + N_C + \propto TSV_{p.u}, \quad (7)$$

where $\propto$ the weight coefficient factor is used to analyze the minimum ($\propto$ =0.5) and maximum ($\propto$ =1.5) importance of the number of components and total standing voltage (TSV). The CF/ N_L gives a balanced approach for different-level topologies.

From Table 3, the proposed topology has better results regarding fewer devices and reduced cost, and it is preferred for renewable energy and electric drive applications.

Table 3

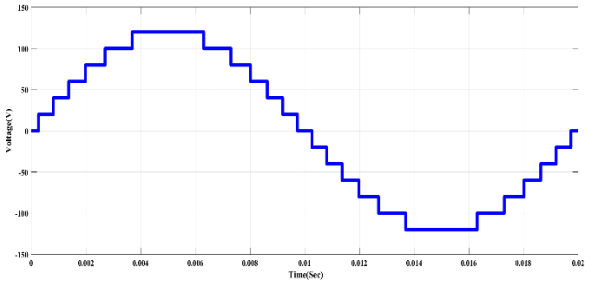
Comparison of performance parameters

Parameters	[8]	[9]	[10]	[11]	[12]	[13]	[14]	[15]	[16]	[P]
N_{DC}	1	1	1	1	1	1	2	2	2	6
N_D	2	1	0	2	0	2	0	2	0	0
Nc	4	3	3	3	3	4	2	2	2	0
N_S	14	14	14	13	15	13	14	13	18	12
N_{GD}	14	14	14	13	15	13	14	13	18	12
CCpL	12.3	5.5	5.7	5.2	5.4	5.3	5.9	5.7	5.5	5.1
TSV	2.7	2.5	2.5	2.5	2.6	2.5	2.8	2.5	3.0	2.3
CF	2.7	2.7	2.9	2.5	2.5	2.5	2.8	2.9	3.1	2.4

CF	3.2	3.3	3.5	3.1	3.2	3.2	3.6	3.5	3.8	2.9	
N_{DC}/ N_L	0.38	0.32	0.32	0.3	0.3	0.3	0.3	6.3	0.3	0.5	
N_{GD} /N_L	1.07	1.08	1.08	1.07	1.1	1	1.0	1	1.3	0.9	
N_S/ N_L	1.07	1.08	1.08	1.07	1.1	1	1.0	1	1.3	0.9	

6. SIMULATION RESULTS

This section is dedicated to the simulation of the proposed 13-level MLI modeled by MATLAB/Simulink to demonstrate the effectiveness of topology under different load scenarios. It consists of 6 sources and 12 switches. The parameters values such as symmetrical voltage source = 20V, peak voltage magnitude (V_{peak}) = 120V, peak current magnitude (I_{peak}) = 12 A resistance (R) = 10 Ω, inductance (L) = 100mH, fundamental frequency (f) = 50 Hz. The output voltage and current waveform for single module 13-level topology are shown in Fig. 4. The Fourier finite analysis (FFT) of total harmonic distortion (THD) for 13-level MLI is illustrated in Fig. 4.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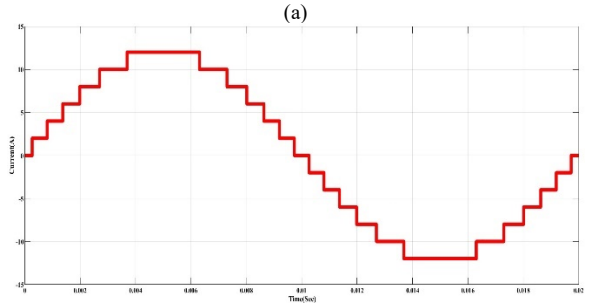
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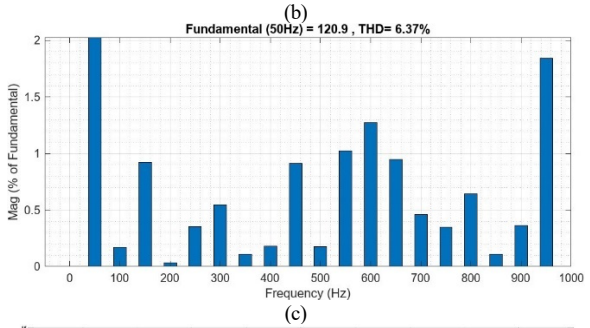

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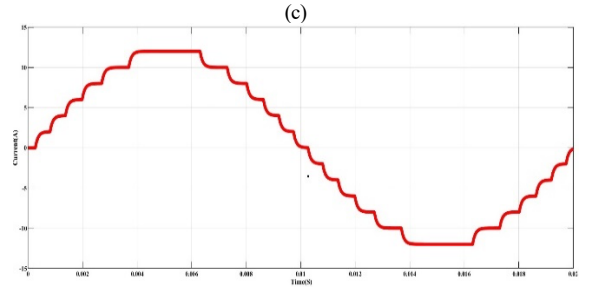
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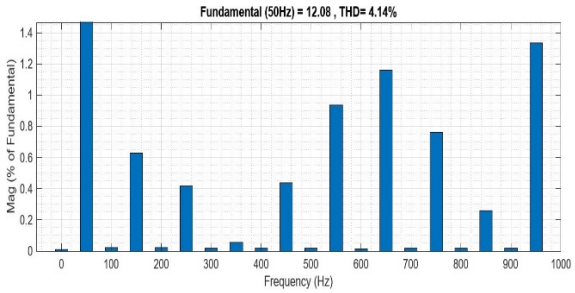
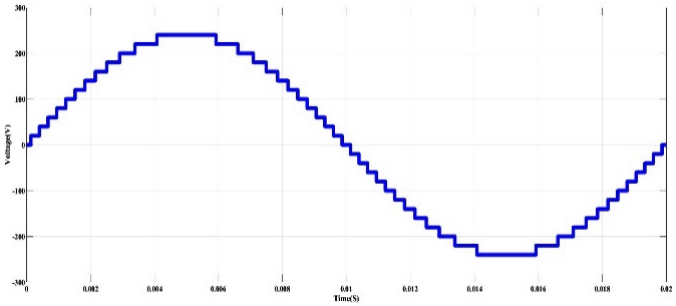


(e)

Fig. 4 – Simulation results of 13-level MLI; (a) output voltage waveform (b) output current waveform for R = 10 Ω; (c) FFT analysis of output voltage waveform for R = 10 Ω. (d) output current waveform for R = 10 Ω and L = 100 mH; (e) FFT analysis of current waveform for R = 10 Ω and L = 100 mH.

Furthermore, the module is cascaded in series; the generalized configuration is implemented to increase the number of levels, which achieves a significant reduction of harmonics. The two-module, 25-level circuit configuration is discussed in this article. The voltage and current waveform for two modules 25-level topology are depicted in Fig. 5. The parameters values such as symmetrical voltage source = 20 V, peak voltage magnitude (V_{peak}) = 240 V, peak current magnitude (I_{peak}) = 24 A resistance (R) = 10 Ω, inductance (L) = 10mH, fundamental frequency (f) = 50 Hz. The THD waveform is shown in Fig. 5.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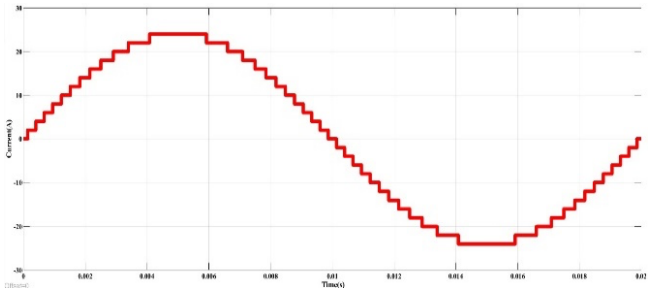
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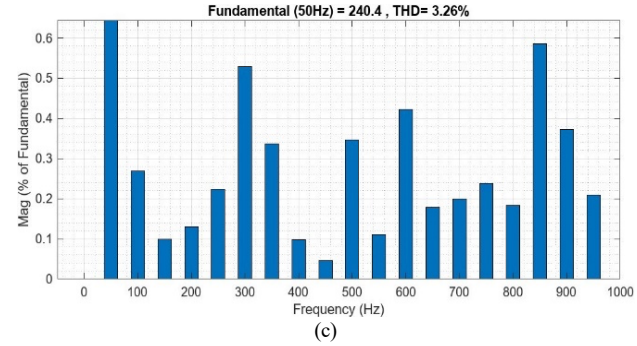

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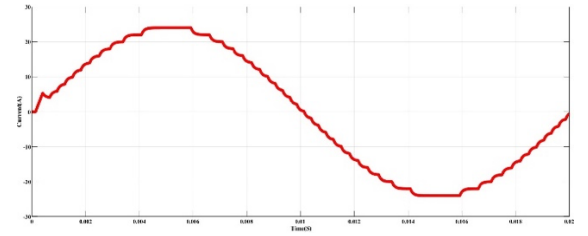

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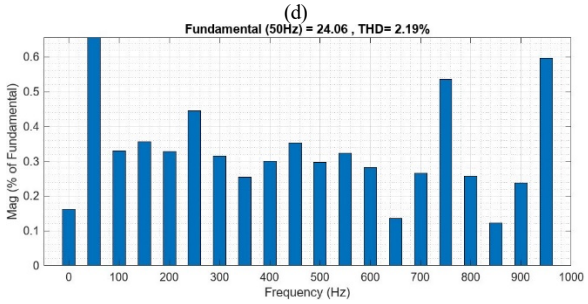
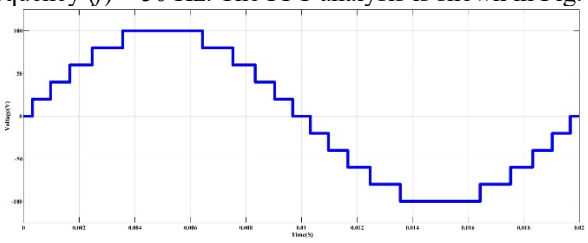


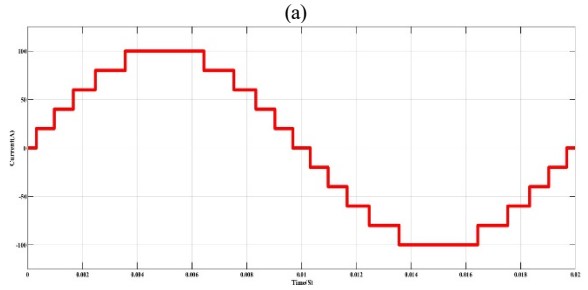
(e)

Fig. 5 – Simulation results of 25-level MLI; (a) output voltage waveform (b) output current waveform for R = 10 Ω; (c) FFT analysis of output voltage waveform for R = 10 Ω. (d) output current waveform for R = 10 Ω and L = 100 mH; (e) FFT analysis of current waveform for R = 10 Ω and L = 100 mH.

The fault-tolerant capability of the proposed topology is also proved by considering the failure of voltage sources. Due to single source failure, the single module 13-level inverter works as an 11-level inverter. It is demonstrated by voltage and current waveform are revealed in Fig. 6. The critical parameters are symmetrical voltage source = 20 V, peak voltage magnitude (V_{peak}) = 100 V, peak current magnitude (I_{peak}) = 10A, resistance (R) = 10 Ω, fundamental frequency (f) = 50 Hz. The FFT analysis is shown in Fig. 6.



(a)



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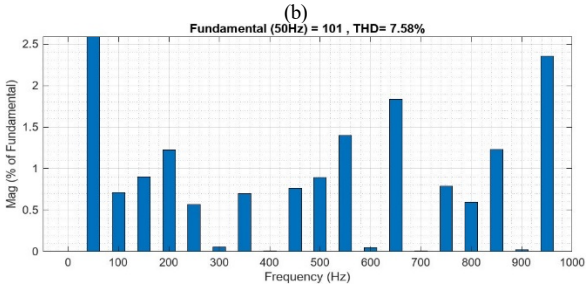

(c)

Fig. 6 – Simulation results of 11-level MLI; (a) output voltage waveform for R = 10 Ω; (b) output current waveform for R = 10 Ω; (c) FFT analysis of 11-level output voltage waveforms for R = 10 Ω.

Table 4 includes detailed information on harmonic values for 13-level, 25-level, and 11-level inverters with different combinations of R and L loads to provide more insight.

Table 4

Load variation analysis of 13-level MLI.

S. No	Load parameters	current THD (%)	voltage THD (%)	Power factor (cos Φ)
1	200mH	0.33%	6.53%	0
2	10Ω & 155 mH	17.78%	6.38%	0.2
3	10Ω & 56 mH	20.89%	6.38%	0.5
4	10 Ω & 24 mH	14.36%	6.43%	0.8
5	10Ω	6.37 %	6.37%	1

Table 5

Load variation analysis of 25-level MLI

S. No	Load	Load current THD (%)	Load voltage THD (%)	Power factor (cos Φ)
1	200mH	0.12%	3.27%	0
2	10Ω & 155 mH	17.75%	3.27%	0.2
3	10Ω & 56 mH	20.80%	3.27%	0.5
4	10 Ω & 24 mH	14.22%	3.29%	0.8
5	10Ω	3.26%	3.26%	1

Table 5

Load variation analysis of 11-level MLI

S. No	Load	Load current THD (%)	Load voltage THD (%)	Power factor (cos Φ)
1	200mH	0.42%	7.63%	0
2	10Ω & 155 mH	18.23%	7.60%	0.2
3	10Ω & 56 Mh	22.12%	7.59%	0.5
4	10 Ω & 24 mH	16.23%	7.61%	0.8
5	10Ω	7.58%	7.58%	1

7. HARDWARE RESULTS

An experiment hardware setup consists of six DC power sources (transformer, diode (UF5408), capacitor (4300 µF), 12 semiconductor switches (IRF460), 12 gate driver circuits (BD140), optocoupler (PC817), Arduino UNO controller, and loads). The hardware prototype model is shown in Fig.7.

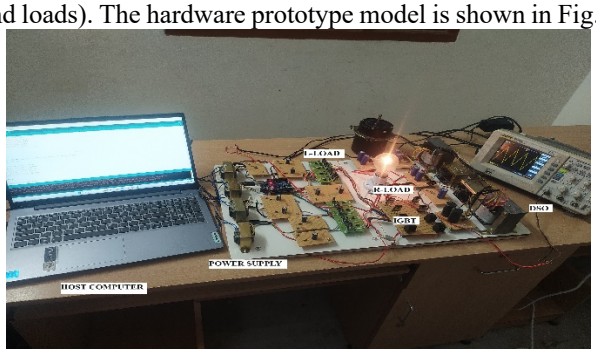

Fig. 7 – Hardware prototype model of MLI.

The individual DC source value is 20V; therefore, the single module has step voltage and peak voltage are 20V and 120V. The 13-level module voltage waveform illustrates in Fig. 8.

Fig. 8 – Hardware result of 13-level MLI.

Similarly, the 25-level inverter output voltage is generated by cascading the two modules of 13-level MLI in series. Figure 9 depicts the 25-level inverter.

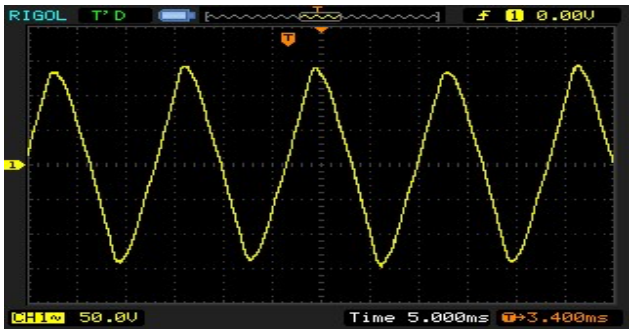

Fig. 9 – Hardware result of 25-level MLI.

8. **CONCLUSIONS**

This article proposes a generalized symmetrical MLI topology with reduced switches and sources. A single module with six symmetrical sources and 12 power switches generates the 13-level voltage waveform. The voltage levels have increased by cascading the module in series, which decreases the harmonic levels but increases the complexity of the circuit. The 2-module MLI produces a 25-level waveform. Then, the fault-tolerant capability of MLI has been discussed due to the failure of voltage sources. The comparison analysis section proves the novelty of circuit configuration with recently published topologies. The NVL modulation technique is used to generate gate pulses. The performance parameter values of 13-level MLI are TSV=2.3, CCpL = 5.1, CF(α = 0.5) = 2.4, CF(α = 1.5) = 2.9, N_{DC}/N_L = 0.5, N_{GD}/N_L= 0.9, N_S/N_L = 0.9, THD (13-level) = 6.37%, THD (25-level) = 3.26%. Furthermore, the detailed simulation results and the hardware prototype model developed in the laboratory validate the waveform outputs under different load conditions. It is well-suited for renewable solar energy systems and electric vehicle applications.

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