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CHAOTIC RANDOMIZED SPACE VECTOR PULSE WIDTH MODULATION INTENDED FOR INDUCTION MOTOR DRIVES IN INDUSTRIAL APPLICATIONS

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In this industrial era, induction motor control plays a vital role, especially in speed control. Adjustment of speed is essential in all control strategies from the application perspective. There are different pulse width modulation methodologies to tune the speed and reduce harmonics. Among various pulse width modulation (PWM) strategies, space vector PWM (SVPWM) proves best for harmonic reduction in drive applications of variable frequency. SVPWM topology is modified by incorporating some randomness, generating switching pulses for the inverter, thereby controlling induction motor drives. A chaotic-based randomized algorithm is synthesized in primitive SVPWM and termed chaotic random SVPWM (CRSVPWM). It is proved from the results that the efficiency and performance are higher for chaotic randomized SVPWM induction drives than all conventional methods of PWM, having higher harmonics, lower modulation index, and less flexibility. CRSVPWM shows the advantages of better fundamental output voltage, more straightforward digital realization, improved harmonic performance, and extreme simplicity in vector selection. It is simulated through MATLAB 2021R, and hardware-based experimental validation was done using the Vivado design suite environment with Spartans-6 FPGA (XC6SLX9-2tqg144).

1. INTRODUCTION

Induction motors (IM), due to their prominent features, it is desired for variable-speed drives, especially in comparison with constant-speed drives. This is due to its reduced manufacturing cost, self-starting, ease of robust construction, and ease of opting for different soft torque-stability control techniques as needed by the modern drive system. Induction machines are the most extensively utilized worldwide just because of what they are called the "workhorse of the industry". The advancements in power electronic switching and developments in semiconductor devices have improved power electronic systems. Space vector pulse width modulation (SVPWM) is a modulation that meets the listed requirements [1]. The induction motor speed control requires a changing voltage and supply frequency, which is continuously gained from the voltage source inverter (VSI) exhibited in Fig.1. Several sorts of pulse width modulation schemes are by varying voltage or frequency, which includes space vector pulse wide modulation, stepped pulse wide modulation, sine wave PWM, random pulse wide modulation, random carrier pulse wide modulation, multiple carrier PWM and third harmonic injection PWM. Out of them, SVPWM shows the privilege of improving performance with higher fundamental voltage [2].

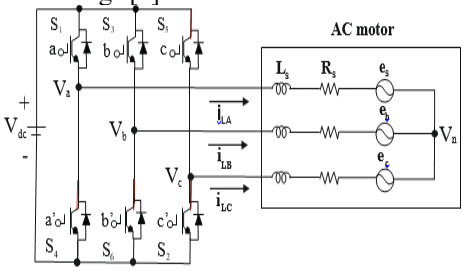

Fig. 1 – Three-phase PWM inverter.

The sinusoidal pulse width modulation (SPWM) and space vector pulse width modulation (SVPWM) are the well-recognized modulation schemes owing to their charming benefits. SVPWM is a computationally intensive algorithm that incorporates the PWM duration calculation algorithm, and it gives the top level of primary voltage when differentiated from SPWM [3–5]. The SVPWM demands fundamental component enhancement and minimal distortion when differentiated from SPWM. Because of higher switching frequency, these two effectively reduce the output voltage with lower-order harmonics. However, the primary component amplitude in SPWM and SVPWM output waveforms is less than that of the rectangular waveform. This represents its lowest performance concerning DC bus utilization. The structure of the three-phase inverter is exhibited in Fig.1. The six PWM signals control the IGBT switches of the inverter.

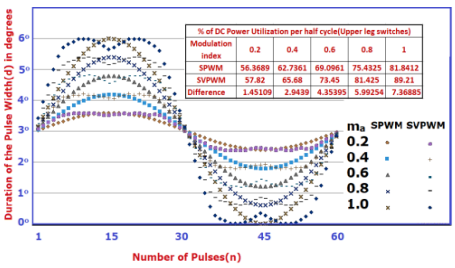

Fig.2 – Pulse width (d) versus pulse number at different m_a for SPWM and SVPWM.

Figure 2 shows the typical changes in pulse width (d) against modulation index function (m_a) for SPWM and SVPWM at a switching frequency of 3 kHz, which exhibits 60 pulses in one 50 Hz fundamental frequency. The observations below have been made from Fig. 2.

1. The width of every pulse varies in proportion to the modulation index for PWM techniques.
2. In SPWM, the pulse widths are maximum at the center of the sine reference wave. In contrast, the upper leg switches pulse widths are maximum when crossing the first sector to the second sector and the second sector to the third sector in the positive half-cycle of the

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SVPWM. Even then, it is moving to the maximum possible pulse width

$$\frac{1}{f_{sw}} \text{ or } \frac{1}{f_{sw}} - \text{dead time.}$$

3. In the negative cycle of the SVPWM, the upper leg switches pulse widths are minimal when crossing the fourth sector to the fifth sector and the fifth sector to the sixth sector. Even then, it is moving to zero or dead time.
4. The duration of the positive pulse and the duration of the negative pulse summation are equal $\frac{1}{f_{sw}}$.
5. In SPWM and SVPWM, the upper leg switch duration in the first half cycle and the lower leg duration in the second half cycle should be the same to avoid even-order harmonics.
6. In SPWM, 81.9% of the pulse width is used at m_a = 1.0, whereas in SVPWM, 89.2% has been used. This is the maximum pulse duration that can be utilized to convert DC to AC. The remaining portions are used as a return path through the opposite leg switches.
7. SPWM and SVPWM can never achieve a cent percent of DC utilization; if they attempt it, it will first become overmodulation, generating dangerous harmonics.
8. When increasing the modulation index, the pulse widths linearly increase when comparing SPWM and SVPWM. That is 1.45 % at m_a = 0.2 and 2.9% at m_a = 0.4. The same scenario continues till the modulation index is 1.0.

This shows the apparent domination of the SVPWM over the SPWM. The drawbacks of the fixed frequency PWM techniques are:

1. The amplitude of the dominating harmonics was present in multiple switching frequencies.
2. The harmonics spreading factor and power spectrum density of inverter output is poor.

These drawbacks can be improved by randomizing the pulse width without de-rating its inherent advantages. Random pulse width modulation (RPWM) is a technique to randomize pulse width. RPWM creation is like normal SPWM, where sinusoidal waves with fixed frequencies are compared. Instead, it is compared to the random carrier [6]. Figure 3 shows the resultant carrier wave with resultant pulses.

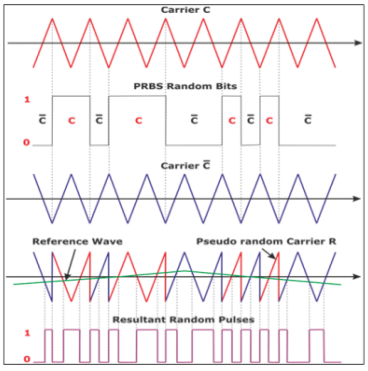

Fig. 3 – Random carrier wave generation.

The carrier waves are given to a mux and as per the set/reset signal provided in the mux the random carrier wave is generated as shown in Fig. 4. Similarly, traditional RPWM randomness can be created on different innovative methods. Among them, a prominent one is a chaotic pulse, where chaos means anything extremely random, like unwanted noise in our appliances, which generates acoustic noise. 16-bit linear feedback shift register has been used to generate the random bits which is shown in Fig.4.

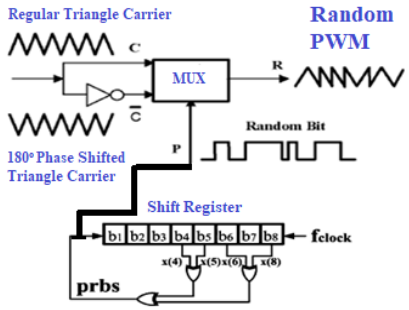

Fig. 4 – Random pulse generation.

Changing the pulse width randomly with SVPWM techniques will give better performance over the fixed frequency SVPWM. This paper presents the chaotic random SVPWM to reduce the THD and spread the harmonics. The chaotic sequence will generate the chaotic frequency, which will modulate the pulse duration of the switches. This PWM in vector control controls the motor output and torque for better dynamic performance, reducing harmonic impacts and improving drive efficiency. Using this vector control along with this new type of randomness will give dynamic performance. Induction motors operate in constant torque and constant speed but are used at variable speeds to improve efficiency in some applications. It can be obtained by variable frequency drives (VFD), which are converters that convert the supply source into AC-AC or DC-AC. A voltage source inverter (VSI) is much more prominent than a current source inverter (CSI). In VSI, the rectified supply is passed through an LC filter, smoothens the converted supply by filtering out the DC output ripples. The filtered wave is again transformed into a quasi-sinusoidal wave using a six-pulse IGBT inverter. The main advantage of VSI is that it provides a high power factor and low harmonic distortion.

The remaining sections of this paper are summarized below. Section 2 describes the phenomena of space vector pulse width modulation with chaotic pulse generation. Section 3 explains the design and implementation of chaotic random SVPWM. Section 4 validates the proposed method by experimental setup. Finally, section 5 concludes the paper.

2. SPACE VECTOR PULSE WIDTH MODULATION

SVPWM is a PWM methodology that has better efficiency than any other PWM technique [7]. It is a switching technique employed in 3-phase PWM VSI exhibited in Fig.1. Power switches S_1 to S_6 are operated by different factors a, b, c. When the upper transistor is in on state, *i.e.* if a, b or c is 1, lower transistors are in off state, i.e. a, b or c is 0. The ON and OFF status of top S_1, S_3 and S_5 transistors always establish output voltage.

The correlation between [a,b,c] the switching vector and [$V_{ab}V_{bc}V_{ca}$] the line - to - line voltage vector is as follows:

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix}. \quad (1)$$

The correlation between variable switching vector [a, b, c] as well as a vector of phase voltage [V_a, V_b, V_c]

could be as follows:

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{V_{dc}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix}. \quad (2)$$

The top three switches have eight possibilities for ON/OFF switching operation. Based on eq. (1) and eq. (2) the switching vectors, voltage velocity, and line-to-line voltage comply with the DC link provided in Table 1, showing voltage at V_0 to V_7 [8–10].

Table 1

Switch vectors, voltages in phase and output line voltages.

Voltage Vectors	Switching Vectors			Line to neutral voltage			Line to line voltage		
	a	b	c	V_{an}	V_{bn}	V_{cn}	V_{ab}	V_{bc}	V_{ca}
V_0	x	x	x	0	0	0	0	0	0
V_1	1	x	x	2/3	-1/3	-1/3	1	0	-1
V_2	1	1	x	1/3	1/3	-2/3	0	1	-1
V_3	x	1	x	-1/3	2/3	-1/3	-1	1	0
V_4	x	1	1	-2/3	1/3	1/3	-1	0	1
V_5	x	x	1	-1/3	-1/3	2/3	0	-1	1
V_6	1	x	1	1/3	-2/3	1/3	1	-1	0
V_7	1	1	1	0	0	0	0	0	0

In SVPWM, the upper three power transistors apply separate switching patterns on the three-phase power inverter. It's proved that voltage or current outputs linked to AC motors have less harmonic distortion than the sinusoidal modulation method [11–13].

The abc reference frame voltage calculations are converted into a static reference frame dq comprising horizontal (d) and vertical (q) indented lines to implement in SVPWM.

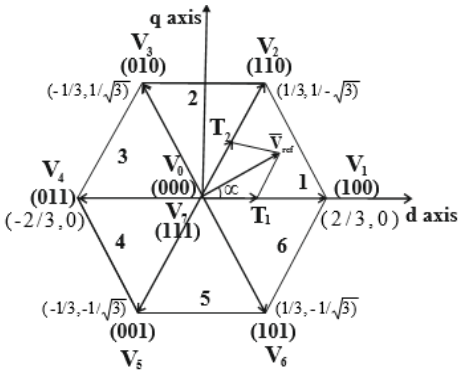

Fig. 5 – Basic vector and sector switching.

As shown in Fig. 5, the non-zero vector (V_1 - V_6) forms a hexagonal. The eight vectors are basic spatial vectors, defined as V_0, V_1, V_2, V_3, V_4, V_5, V_6 and V_7. The purpose of the PWM vector is to estimate the references of the voltage vector used by the eight-way shift [11,14–16].

The following procedures can be used for implementing SVPWM:

a) Specify V_{ref} ,V_d, V_q and angle (α)
b) EvaluateT_1, T_2, T_0time
c) Evaluate each transistor's switching time (S_1 to S_6)

2.1. TOTAL HARMONIC DISTORTION (THD)

THD is a commonly known term in the analysis of harmonics. It is the measure of proximity with a clean sine wave to an original waveform. THD is zero for pure sine wave. It is expressed as

$$THD = \sqrt{\sum_{n=2}^{m} \left(\frac{V_n}{V_1}\right)^2} \times 100\% = \frac{\sqrt{\sum_n^m -2{V_n}^2}}{V_1} \times 100\%, \quad (3)$$

where V_1 is the basic harmonic voltage rms, and V_n is the the tenth-order harmonic voltage RMS.

2.2. HARMONIC SPREAD FACTOR: IT IS A SPECIFIC INDEX FOR CALCULATING THE SPREADING HARMONICS IN A WAVEFORM.

$$HSF = \sqrt{\frac{1}{n}} \sum_{k=0}^{n} \left(H_j - H_0\right)^2, \quad (4)$$

$$H_0 = \frac{1}{n} \sum_{j>1}^{n} H_j \,(1.3). \quad (5)$$

Here 'H_j' amplitude of j^{th} harmonics. For all 'n' harmonics, 'H_0' is an average [17,18].

3. PROPOSED STRATEGY-CHAOTIC RANDOM SVPWM IMPLEMENTATION

From the previous section, it is clear how the chaotic sequence is applied to the normal SVPWM. To recount, the switching frequency obtained from the chaotic sequence is taken to find the total switching period, which will be the total switching time for the gate pulses of the IGBT inverter. This period is then given to the SVPWM technique, generating corresponding pulses. Figure 6 shows the proposed method for chaotic, random SVPWM implementation.

The comparison of THD of different PWM techniques is also considered. Here, MATLAB 2018 is used to simulate the chaotic SVPWM.

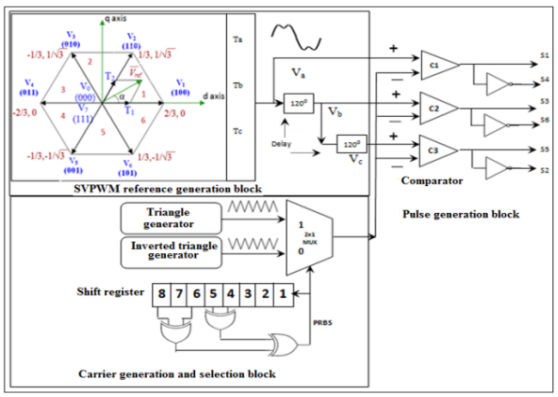

Fig. 6 – Proposed strategy-chaotic random SVPWM

3.1 CHAOTIC RANDOM SVPWM: SIMULATION

The proposed chaotic random SVPWM (CRSVPWM) is incorporated with the indirect field-oriented control (IFOC), as shown in Fig. 7. The motor needs a rotor position feedback device and sensors to track the 3ϕ stator currents. For this purpose, an encoder is typically installed on the shaft rotor. An explanation of the coordinate reference transformation procedure is essential to comprehending the operation of vector control. From its point of view, a sinusoidal input current is driven into the stator. A rotating magnetic flux is generated because of this time variation signal. The rotating flux vector determines the rotor's speed. When seen from a stationary position, the stator currents, motor, and spinning flux vector appear to be AC quantities. The simulation of CRSVPWM is simulated as shown in Fig. 8. Here, a range of minimum frequency F_low and maximum frequency F_high is taken as high values ranging from 9000 – 10000 to avoid ripples in the low-frequency range. C is an arbitrary value and is taken as 6. By the constraints provided, the result obtained is,

$$F_s = 1.1157e^{+06}, \quad (6)$$

$$T_s = 8.9632e^{-07}. \quad (7)$$

Now the switching time obtained can be varied by varying the constraints. The total switching period is obtained from the chaotic sequence.

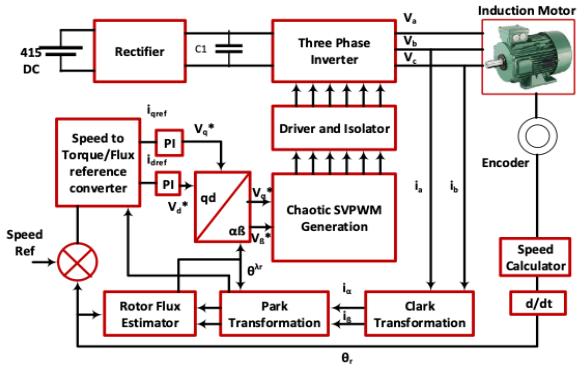

Fig. 7 – Block diagram of IFOC scheme incorporated with the proposed chaotic SVPWM.

3.2 CALCULATION OF MODULATION INDEX m_a, THETA, SECTOR, AND SWITCHING PULSE GENERATION

There are six sectors in the hexagon. The sector calculation is as follows:

$$\begin{cases} 0 \le \theta \le 60 & ; \text{Sector 1} \\ 60 \le \theta \le 120 & ; \text{Sector 2} \\ 120 \le \theta \le 180 & ; \text{Sector 3} \\ -180 \le \theta \le -120 & ; \text{Sector 4} \\ -120 \le \theta \le -60 & ; \text{Sector 5} \\ -60 \le \theta \le 0 & ; \text{Sector 6} \end{cases} \quad (8)$$

The equations are the same as those discussed earlier. Instead, T_1, T_2, and T_0 are named T_a, T_b, and $T_0/2$. T_s is obtained from the chaotic sequence, and n is taken as a sector.

$$T_a = MI \times \sqrt{3} \times \frac{T_s}{\pi} \sin\left(\frac{n}{3}\pi - \theta + 2\pi f t\right), \quad (9)$$

$$T_b = MI \times \sqrt{3} \times \frac{T_s}{\pi} \sin\left(\theta + 2\pi f t - \frac{(n-1)}{3}\pi\right). \quad (10)$$

The total time T_z is taken as $T_s/2$ thus T_0 is,

$$\frac{T_0}{2} = \frac{T_s}{2} - T_a - T_b. \quad (11)$$

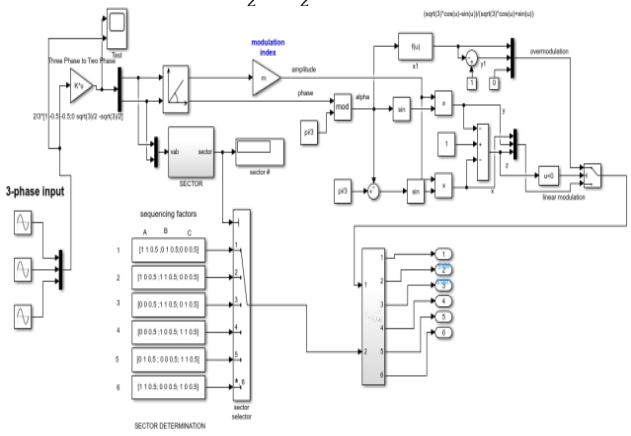

Fig. 8 – Generation of random SVPWM in MATLAB.

Transition changes are calculated from T_b and T_0 / 2. The chaotic pattern is embedded in the script. Figure 9 shows the inverter output line-to-line voltage waveform (low pass filtered) with SVPWM sector 1-PWM gate pulses.

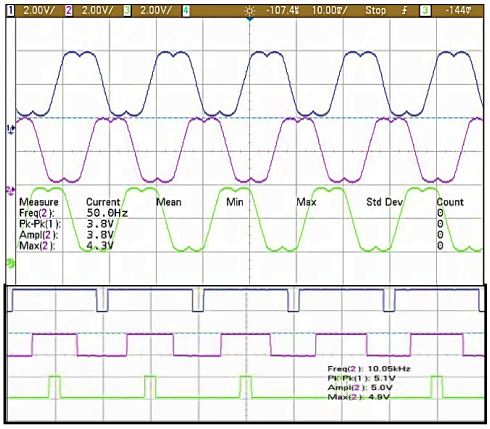

Fig. 9 – Inverter output line-to-line voltage waveform (low pass filtered) with SVPWM-sector 1 PWM gate pulses.

3.3 PERFORMANCE COMPARISON

The performances of other PWM methods are compared with the advanced chaotic SVPWM (Table 2). The above DC voltage (V_{DC}) is 415 V; thus, the output frequency is taken as 50 Hz.

Table 2

Comparison result: output voltage.

Modulation Index (ma)	Output Voltage (V)		
	RCPWM	CPWM	CRSVPWM
0.2	74.2	75	75.3
0.4	135.5	136.8	137.2
0.6	210.3	211	211.3
0.8	293.2	294	294.2
1.0	366.7	367	367.4

Table 3

Comparison result: THD.

Modulation Index (Ma)	THD (%)		
	RCPWM	CPWM	CRSVPWM
0.2	241.9	241.0	240.8
0.4	168.0	168.0	167.8
0.6	122.2	122.0	122.0
0.8	89.2	89	88.9
1.0	66.7	66.2	66

Table 4

Comparison result: harmonic spread factor.

Modulation Index (Ma)	HSF		
	RCPWM	CPWM	CRSVPWM
0.2	7.1	5.2	4.6
0.4	5.9	4.7	4.4
0.6	5.6	4.6	4.2
0.8	5.2	4.1	3.9
1.0	4.7	3.7	3.5

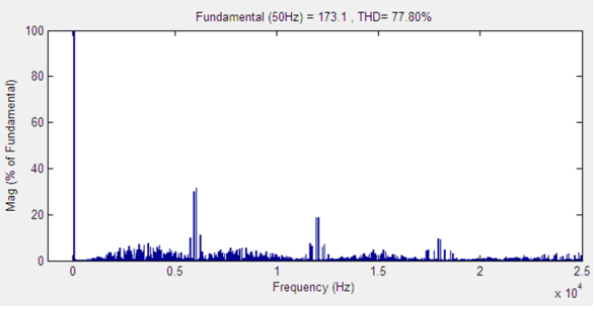

Fig. 10 – Line to line voltage and its spectrum-FFT.

Comparing the THD of RCPWM, CPWM, and

CRSVPWM techniques reveals that the THD of chaotic random SVPWM is less than that of all existing methods (Table 3 and Table 4). Figure 10 shows the inverter output line-line voltage spectrum at modulation index m_a = 0.8. It indicates that harmonics are distributed across the band of one clock cycle.

3.4 HARDWARE VALIDATION

Figure 11 demonstrates the proposed experimental framework for implementing the developed CRSVPWM. It has a rectifier, diode, three-phase VSI (1200 V, 25 A, and 20 kHz Mitsubishi Smart Module), PC, Spartans-6 FPGA (XC6SLX9-2tqg144), and host storage. Field-programmable gate arrays (FPGAs) implement digital circuits, and their specifications are tabulated in Table 5. The programmability of FPGAs permits all circuits to be composed immediately by appropriate programming [17].

Table 5

Hardware Specification

DC input voltage:	V_{DC} = 415 V
Basic frequency:	f= 50 Hz
Index of the modulation:	m_a = 0.8
Switching frequency:	fz= (3,-3) kHz
Random number generator:	PRBS (8 bit)
Motor load:	(0.75 kW & 2.5 A)

Using Xilinx Vivado design suite 2017.1 synthesizer and VHDL language-based, register transfer Level (RTL) architectures are used to implement chaotic random SVPWM. Table 6 specifies the comparisons between the test results and the hardware for CRSVPWM. The experimental results were found to be closely related to the simulation. Table 7 shows the dynamic and no-load results of the proposed scheme with filters. It gives better results when compared without filters.

Table 6

Comparison of simulation and hardware results.

Modulation Index (Ma)	Results for simulation		Results of Hardware	
	Voltage output (V)	THD (%)	Voltage output (V)	THD (%)
0.2	75.3	240.8	74	243
0.4	137.2	167.8	136	169
0.6	211.3	122.0	210	123
0.8	294.2	88.9	293	89
1.0	367.4	66	366	68

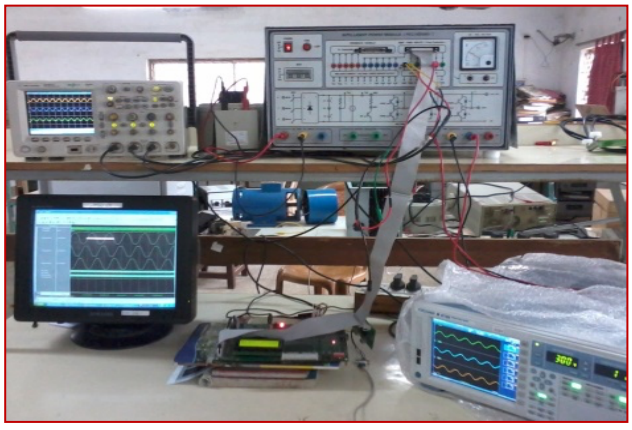

Fig. 11 – Experimental setup.

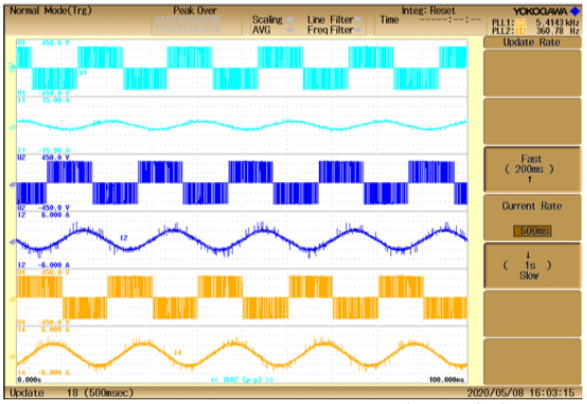

Fig. 12 – Output line voltage and current waveform (m_a = 0.8)

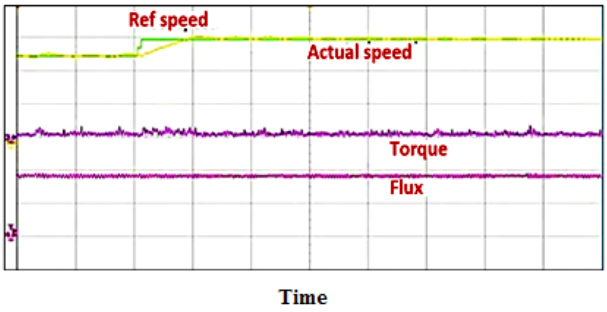

Fig. 13 – Shifting of speed from 1200 rpm to 1400 rpm, flux, and torque (X-axis: 200 ms/div; Y-axis: Speed: 2 v/div = 400 rpm).

Table 7

RMS values of voltage, current, and THD

Response	I_{rms} (A)	V_{rms} (V)	I_{THD} (%)	V_{THD} (%)
No load Response	0.8704	389.90	3.141	7.115
Dynamic response	1.8108	380.74	3.897	9.847

Table 8

Analysis of dominating harmonics order.

Dominating harmonics for m_a = 0.8					
CRPWM		CPWM		CRSVPWM	
DHO	% of Magnitude (Fundamental)	DHO	% of Magnitude (Fundamental)	DHO	% of Magnitude (Fundamental)
56	13.2	60	10.51	115	11.61
58	18.65	119	38.26	119	31.45
62	18.7	121	40.07	121	30.3
119	30.91	167	9.98	239	18.3
121	30.76	239	12.72	241	18.82
239	18.7	241	13.91	359	9.4
241	18.6	245	10.69	361	9.1
Other Harmonic Orders	<10	Other Harmonic Orders	<10	Other Harmonic Orders	<10

For the entire inverter output measurements, Yokogawa digital storage oscilloscope has been used. Figure 12 exhibits voltage in line-to-line and phase voltages of the phase inverter. Modelsim SE-6410.6d software was used to verify the functionality of the VHDL design. The following observations are made from the simulation and experimental analysis:

(i) The essential advancement of CRSVPWM is 0.43% higher than RCPWM and 28.14% higher than CPWM for modulation index 1.0. In CRSVPWM, 0.22% of THD is reduced by differentiating with RCPWM, and 24.89% is reduced when differentiated with CPWM for modulation index 1.0.

(ii). A perceptible dominating harmonic order affects the

operation of the inverter-fed drives framework.

(iii) Multiple harmonic clusters ($2f_c$ = order 62, 58, and 56) exist in the harmonic spectrum of CRSVPWM and RCPWM ($2f_c$=order 60), whereas these have lower than 5% magnitude in CRSVPWM which are shown in Table 7 as well as Fig. 12.

(iv) On real-time realization, the XC6SLX9-2tqg144, 45 nm low-cost FPGA device is employed, and the least FPGA resources have been used in continuation of that least power dissipated by FPGA. The IM was used to begin the test at a predetermined speed of 1200 rpm. 1400 rpm was added to this. It took 0.25 seconds to settle the response. Figure 13 shows the step response to torque, flux, and speed. During the speed shift from 1200 to 1400 rpm, the flux generated remained constant and was not affected by speed. It didn't change across the entire speed range. Additionally, the torque was continuous across the whole speed range.

4. CONCLUSION

This study proposes the CRSVPWM technique, which is an upgrade over conventional fixed-frequency PWM in a three-phase inverter. The detailed harmonic analysis, along with THD and HSF reports, evidence the proposed scheme. This scheme is implemented in real-time using Spartan XC6SLX9-2tqg144 FPGA with a three-phase motor induction squirrel load. The proposed scheme can be extended with modern three-phase multilevel inverters with closed-loop control.

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