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NOVEL SHUNT ACTIVE POWER FILTER BASED ON NINE-LEVEL NPC INVERTER USING MC-LSPWM MODULATION STRATEGY

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Keywords: Nine-level neutral point clamped inverter; Shunt active power filter; Power quality improvement; Multi-carrier level-shifted sinusoidal pulse width modulation strategy (LS-SPWM); Total harmonic distortion (THD).

This paper presents a novel shunt active power filter (Shunt APF) system based on a nine-level neutral point clamped (NPC) inverter, which can reduce current harmonics under various nonlinear loads. These loads can introduce harmonic currents within the system, which causes excessive power losses and alters the voltage systems' characteristics. Today, multi-level inverters are more suitable for high-voltage applications; their advantages are low harmonic distortions, low switching losses, low electromagnetic interference, and low acoustic noise. The reference signals required to compensate harmonic currents use the synchronous detection method (SDM) with phase disposition sinusoidal pulse width modulation (PD-SPWM) control due to its low complexity and superior performance. The proposed shunt APF configuration simulation is evaluated using MATLAB-Simulink and SimPowerSystem environment with inductive and capacitive non-linear loads. The simulation results show the efficiency of the proposed shunt APF in terms of harmonic compensation and power quality improvement. The results of comparative studies with other less multi-level inverters confirm the superiority of the proposed shunt APF system.

1. **INTRODUCTION**

The negative impact of nonlinear loads on the operation of a power grid is widely known and has been confirmed by many studies [1,2]. Passive filters can improve the performance of distribution systems, but problems like the possibility of occurring series or parallel resonance led researchers to active power filters [3]. Active power filters have been proposed as an interesting and high-performance solution to improve power quality [4,5]. These systems are frequently used to suppress power quality problems because they use the technology of power-electronic circuits incorporating power-switching devices and passive energy-storage elements with sophisticated control techniques [6]. The shunt active power filter (shunt APF) is widely used to eliminate the current distortion [7].

A series active power filter is a control device that feeds modern industry with a high-quality power supply [8]. A coupling transformer is inserted in a series between the load and the ac power source voltage. It can significantly improve power quality and ensure a reliable voltage supply to the load by mitigating or eliminating issues such as voltage distortions, sags, swells, and unbalances [9]. Conventional voltage source inverters (2L-VSIs) are widely used in low-voltage applications [10], usually operated at very high switching frequencies. However, high switching frequency leads to high switching losses, electromagnetic emission, and d*v*/d*t* stress [11].

These problems can be solved by adopting multi-level inverters (MLIs) with low switching frequency [12]. The neutral-point-clamped (NPC) converter topology has received more attention and has been extensively used in numerous applications [13,14], including medium- and high-voltage electric motor drives, static compensators (STATCOMs), and another utility type of power electronic systems for almost three decades now [15,16]. These multi-level (NPC) converters employ clamping diodes and series dc capacitors to produce ac voltage waveforms with multiple advantages: lower voltage harmonics on the alternative current side, smaller filter size, lower switching losses, lower electromagnetic interference, lower voltage stress on the semiconductor devices and lower acoustic noise. These advantages can reduce the construction cost of active filters in medium and high-voltage applications [17]. Most research has focused on converters with three or five voltage levels, although topologies with many voltage levels were also proposed [18]. In general, the higher the voltage levels of the converter, the less harmonic and better the power quality, but it increases the circuit and control complexity [19].

The modulation strategy of multilevel inverters aims to synthesize the output voltage as close as possible to the sinusoidal waveform [20]. Control techniques have been developed to reduce harmonic and minimize the switching loss. Various pulse width modulation (PWM) strategies are available for multilevel converter applications [21]. A carrier-based pulse width modulation (CB-PWM) technique is the natural extension of the conventional two-level sinusoidal pulse width modulation (SPWM) method [22]. It is generally classified into the phase disposition (PD), phase opposition disposition (POD), and alternate phase opposite disposition (APOD) categories. The PD-PWM is much better than POD-PWM and APOD-PWM in waveform shape and THD of the output line voltages. In CB-PWM, (n-1) carrier signals are required, where n is the line-to-line number of levels [23]. The control strategy generates reference signals for shunt APFs. The compensation effectiveness depends on its ability to follow the reference signals with minimum error and time delay. In this work, the synchronous detection method (SDM) is adopted. It is easy to implement and achieve effective compensation for the current harmonic.

The paper presents a novel shunt APF configuration based on a nine-level (NPC) inverter with a multicarrier level shifted pulse width modulation (MC-LSPWM) strategy capable of compensating harmonic currents and improving the power quality. It is structured as follows. The description of the shunt APF is presented in section 2. The nine-level (NPC) inverter is given in section 3. The control strategy is addressed in section 4. The switching pulse generation for the nine-level (NPC) inverter using a multi-carrier level-shifted modulation strategy is described in section 5. The simulation results and discussions are presented in section 6. Finally, the paper concludes by summarizing the principal obtained results and references list.

2. **SHUNT ACTIVE POWER FILTER CONFIGURATION**

Figure 1 shows the bloc diagram of the proposed shunt active power filter. The nine-level inverter can produce an

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output voltage with much less switching frequency ripple than the conventional voltage source inverter (VSI). The configuration is controlled to cancel current harmonics on the AC side and make the source current in phase with the voltage source.

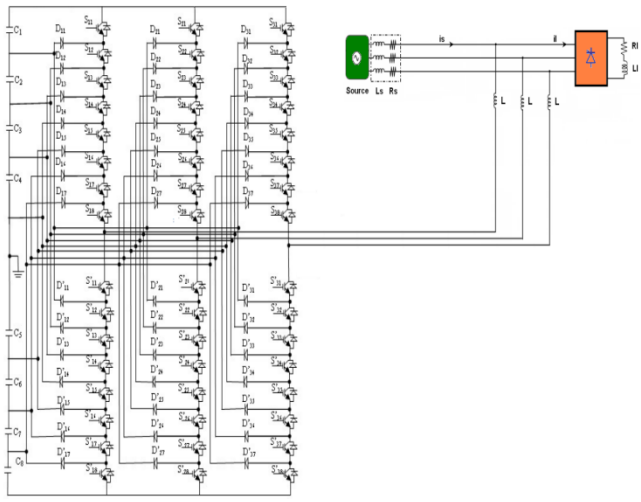


Fig. 1 – Shunt active power filter based on a nine-level (NPC) inverter.

3. NINE-LEVEL (NPC) INVERTER

In recent years, multilevel converters have been widely used and have shown some significant advantages compared to conventional voltage source inverters (VSI) [24], especially for high-power and high-voltage applications. The nine-level inverter is most suitable as compared to the conventional. In addition to their superior output voltage quality, they can reduce voltage stress across switching devices. Since the output voltages have multiple levels, lower is achieved, which greatly alleviates electromagnetic interference problems due to high-frequency switching [25].

Over the past years, different research works have focused on multi-level voltage converters; the more voltage levels there are, the less harmonic and better power quality they provide. However, this improvement is accompanied by an increase in converter complexity. It has been shown that although more voltage levels generally mean lower total harmonic distortion (THD), the gain in THD is marginal for converters with more than seven levels. The conventional three-phase (NPC) n-level inverter based on voltage source will need several (n-1) dc-link capacitors, 2(3n-3) switches, and (6n-12) diodes-clamped (despite anti-parallel diodes of inverter switches). This inverter's maximum voltage across each capacitor equals $U_{dc}/(n-1)$ [26]. Figure 2 illustrates different bloc diagram inverters with two, three, and N levels.

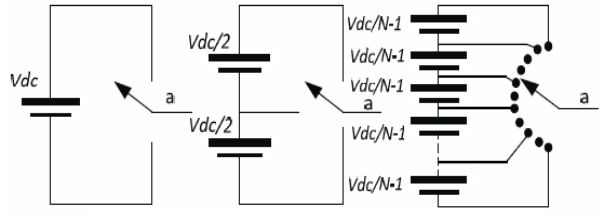


Fig. 2 – Multi-level inverters with 2, 3, and *N* levels.

Figure 3 shows the nine-level (NPC) inverter block diagram. It comprises three arms, each with sixteen IGBTs noted as "Sij". The index (i) indicates the phase: if i=1, it means phase "A," i = 2 the phase "B," and i = 3 phase "C."

The index (j) indicates the number of the switches noted as Si1, Si2, Si3, Si4, Si5, Si6, Si7, and Si8 form the upper part of the arm in each phase, and the switches noted as S'i1, S'i2, S'i3, S'i4, S'i5, S'i6, S'i7, and S'i8 form the lower part of the arm in each phase [27]. The switches should not be simultaneously opened or closed to prevent the short circuit of the dc source of the inverter input. The dc bus capacitor is split into eight, providing four neutral points per phase. Each switch consists of a transistor with a diode in anti-parallel and forty-two clamping diodes connected to the neutral point; these clamping diodes are used to block the reverse voltage and create the connection with the point of reference to obtain midpoint voltages.

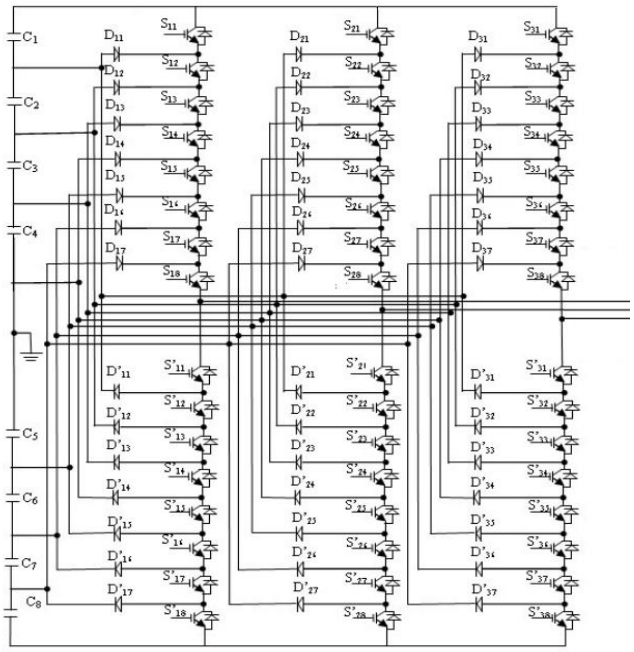


Fig. 3 – Nine-level (NPC) inverter.

The switching states of the nine-level (NPC) inverter are given in Table 1.

Table 1

Switching states of nine-level (NPC) inverter

	Sij	A	B	C	D	0	E	F	G	H
Switch-ing states	Si1	1	0	0	0	0	0	0	0	0
	Si2	1	1	0	0	0	0	0	0	0
	Si3	1	1	1	0	0	0	0	0	0
	Si4	1	1	1	1	0	0	0	0	0
	Si5	1	1	1	1	1	0	0	0	0
	Si6	1	1	1	1	1	1	0	0	0
	Si7	1	1	1	1	1	1	1	0	0
	Si8	1	1	1	1	1	1	1	1	0
	Si'1	0	1	1	1	1	1	1	1	1
	Si'2	0	0	1	1	1	1	1	1	1
	Si'3	0	0	0	1	1	1	1	1	1
	Si'4	0	0	0	0	1	1	1	1	1
	Si'5	0	0	0	0	0	1	1	1	1
	Si'6	0	0	0	0	0	0	1	1	1
	Si'7	0	0	0	0	0	0	0	1	1
	Si'8	0	0	0	0	0	0	0	0	1
Output voltages Udc		+1 E/2	+3 E/8	+2 E/8	+1 E/8	0	-1 E/8	-2 E/8	-3 E/8	-1 E/2
Tk		4	3	2	1	0	-1	-2	-3	-4

In this topology configuration, nine output voltage levels can be obtained: $+4U_{dc}/8$, $+3U_{dc}/8$, $+2U_{dc}/8$, $+U_{dc}/8$, 0, $-U_{dc}/8$, $-2U_{dc}/8$, $-3U_{dc}/8$ and $-4U_{dc}/8$ corresponding to nine switching states A, B, C, D, 0, E, F, G and H [28]:

- Van = Udc/2; switches S1, S2, S3, S4, S5, S6, S7, and S8 are closed.
- Van = 3Udc/8, switches S2, S3, S4, S5, S6, S7, S8, and S'1 are closed.
- Van = 2Udc/8, switches S3, S4, S5, S6, S7, S8, S'1, and S'2 are closed.
- Van = Udc/8, switches S4, S5, S6, S7, S8, S'1, S'2, and S'3 are closed.
- Van = 0, switches S5, S6, S7, S8, S'1, S'2, S'3, and S'4 are closed.
- Van = –Udc/8 switches S6, S7, S8, S'1, S'2, S'3, S'4, and S'5 are closed.
- Van = –2Udc/8 switches S7, S8, S'1, S'2, S'3, S'4, S'5, and S'6 are closed.
- Van = –3Udc/8 switches S8, S'1, S'2, S'3, S'4, S'5, S'6, and S'7 are closed.
- Van = –Udc/2; switches S'1, S'2, S'3, S'4, S'5, S'6, S'7, and S'8 are closed.

4. CONTROL STRATEGY

The harmonic current compensation strongly depends on the performance of the chosen extraction reference current method [29], and the efficiency of the APF functioning depends on its control system that generates switching pulses for the power switches. In this work, we chose the synchronous detection method, a time domain harmonic detection method introduced to calculate the reference currents instantaneously [30] with few calculations. In this method, it is assumed that three-phase source currents are balanced after compensation, the compensating currents of the active filter are calculated by sensing the load currents, the current delivered by dc voltage regulator I^*_{smd}, peak voltage of ac source (V_{sm}) and zero crossing point of source voltage [31]:

$$\begin{aligned} V_{sa}(t) &= V_{sm}\sin(\omega t), \\ V_{sb}(t) &= V_{sm}\sin(\omega t + \tfrac{2\pi}{3}), \\ V_{sc}(t) &= V_{sm}\sin(\omega t + \tfrac{4\pi}{3}). \end{aligned} \quad (1)$$

The average active power of the alternative current source must be equal to P_{Lav} and can be calculated as:

$$P_s = \frac{3}{2} V_{sm} I^*_{smp} = P_{Lav}. \quad (2)$$

From eq. (2), the first component of the alternative current side can be calculated:

$$I^*_{smp} = \frac{2}{3} P_{Lav}/V_{sm}. \quad (3)$$

The second component of ac source current I^*_{smd} is obtained from proportional-integral capacitor voltage regulator. The required peak source current I^*_{sm} can be calculated using equation (4):

$$I^*_{sm} = I^*_{smp} + I^*_{smd}. \quad (4)$$

The ac source currents must be sinusoidal and in phase with source voltages:

$$\begin{aligned} i_{ua}(t) &= V_{sa}/V_{sm}, \\ i_{ub}(t) &= V_{sb}/V_{sm}, \\ i_{uc}(t) &= V_{sc}/V_{sm}. \end{aligned} \quad (5)$$

The reference source currents can be obtained from

$$\begin{aligned} i^*_{sa}(t) &= I^*_{sm}.i_{ua}(t), \\ i^*_{sb}(t) &= I^*_{sm}.i_{ub}(t), \\ i^*_{sc}(t) &= I^*_{sm}.i_{uc}(t). \end{aligned} \quad (6)$$

The compensation currents of the shunt active power filter can be obtained from (7):

$$\begin{aligned} i^*_{ca}(t) &= i^*_{sa}(t) - i_{La}(t), \\ i^*_{cb}(t) &= i^*_{sb}(t) - i_{Lb}(t), \\ i^*_{cc}(t) &= i^*_{sc}(t) - i_{Lc}(t). \end{aligned} \quad (7)$$

To include switching and converter losses, additional loss component of current will be added using a proportional integral voltage controller to regulate the dc link voltage U_{dc} [32]. The control loop consists of the comparison of the measured voltage U_{dc} with the reference voltage U_{dc-ref}. The loop generates corresponding current I_{c-loss} given by:

$$I_{c-loss} = K_p \Delta U_{dc} + K_i \int \Delta U_{dc}\, dt. \quad (8)$$

Figure 3 illustrates the diagram block of the control strategy based on the synchronous detection method.

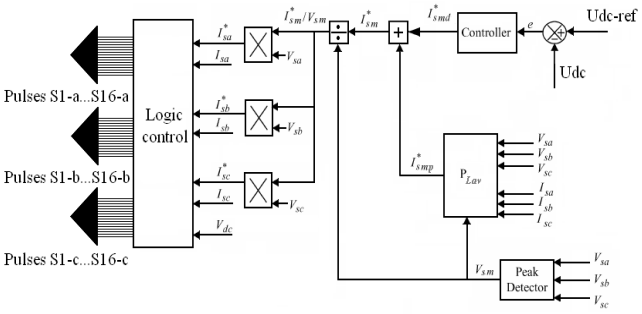


Fig. 3 – Synchronous detection method.

5. SWITCHING LOGIC CONTROL

The difference between the injected and reference currents determines the reference signals. These signals are compared with eight triangular-carrying identical waves shifted from one to the other by a (+4Upm +3Upm +2Upm +Upm, –Upm –2Upm –3Upm and –4Upm) for generating the switching pulses. If the reference signal is larger than the carrier, the output is 1 and 0 otherwise [33]. The quantities T_k are used to determine the output voltage; the maximum output voltage is obtained with T_k equal to 4, and the minimum value is obtained when T_k equals –4.

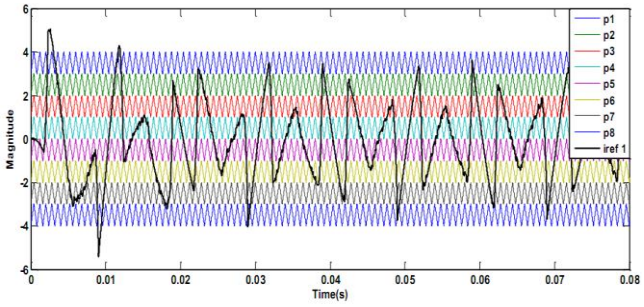


Fig. 4 – Nine-level (NPC) inverter: MC-level shift SPWM modulation.

The forty-eight (48) switching signal pulses of the nine-level (NPC) inverter are generated by comparing the compensating currents with the reference currents using the MC-SPWM modulation strategy respecting the algorithm given by Table 2.

Table 2

Nine-level (NPC) inverter switching generation

Algorithm: Nine-level (NPC) inverter switching generation			
If	Vref1 >= Vpj	Then	Tk1j=1
If	Vref1< Vpj	Then	Tk1j=0
If	Vref1 <= Vpj+4	Then	Tk2j=1
If	Vref1 > Vpj+4	Then	Tk2j=0
K= 1, 2, 3 and j= 1, 2, 3, 4			
TK= (Tk11-Tk21) + (Tk12-Tk22) + (Tk13-Tk23)			
If	TK= 4	Then	VK= +Udc/2
If	TK= 3	Then	VK= +3Udc/8
If	TK= 2	Then	VK= +2Udc/8
If	TK= 1	Then	VK= +Udc/8
If	TK= 0	Then	VK= 0
If	TK=-4	Then	VK= -Udc/2
If	TK=-3	Then	VK= -3Udc/8
If	TK=-2	Then	VK= -2Udc/8
If	TK=-1	Then	VK= -Udc/8

The Simulink switching pulses generation model of a nine-level (NPC) inverter in the case of $T_k = 3$ is shown in Fig. 5.

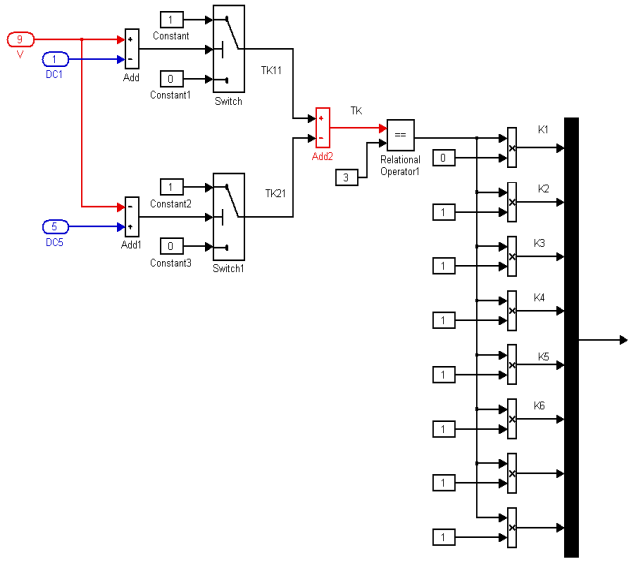


Fig. 5 – Nine-level (NPC) inverter switching pulses generation for the upper leg in case of $T_k = 3$ (T_k:–4,–3,–2,–1,0,1,2,3,4).

6. SIMULATION RESULTS AND DISCUSSION

The simulation results are provided to verify the performance and effectiveness of the proposed Shunt APF under different mode operations with inductive and capacitive non-linear loads. The MATLAB/Simulink model of the novel configuration of a shunt active power filter based on the nine-level (NPC) inverter is presented in Fig. 6. It is composed mainly of the three-phase supply sources, nine-level (NPC) converter, a nonlinear load (rectifier & R, L or R, C) and LS-SPWM controller; measuring blocks are incorporated to measure respective voltages and currents. The simulation parameters are presented in Table 3.

Table 3

Simulation parameters

Source supply	Non-linear loads	Nine-level (NPC) shunt APF
Vs=220 V/50 Hz Rs= 0.1 mΩ Ls= 20 mH	Lf =3 mH	Udc-ref =800 V C1=C2= C3= C4= C5= C6= C7= C8=3000 µF Fs(switching frequency= 10 kHz)

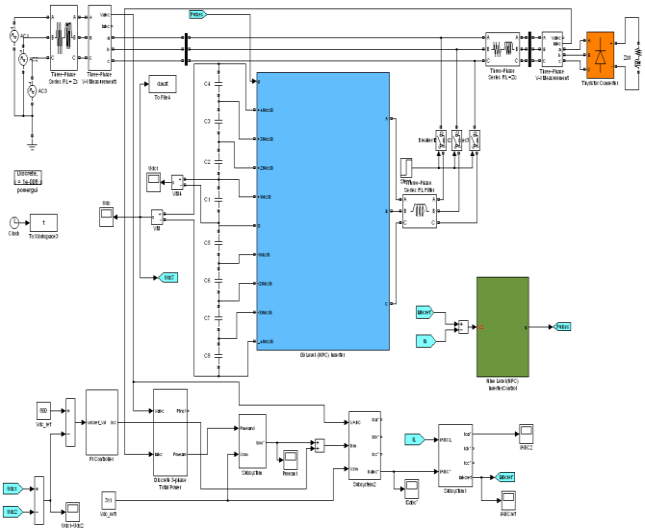
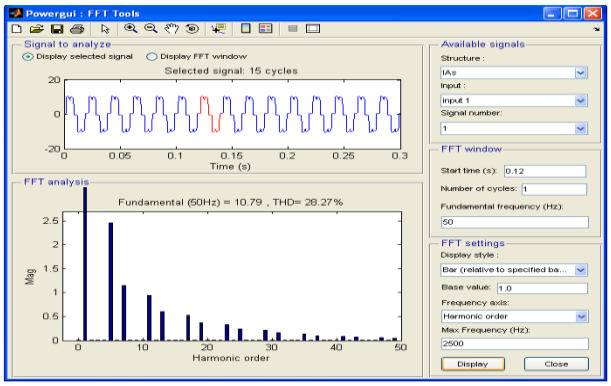


Fig. 6 – Shunt APF simulation model based on a nine-level (NPC) inverter.

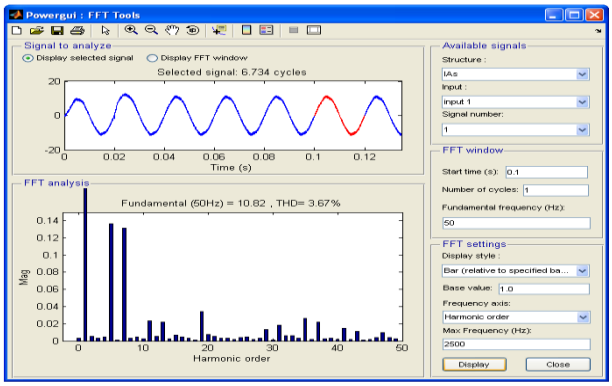
6.1. HARMONIC CURRENT COMPENSATION

Before compensation, the source current shown in Fig. 7 is distorted with a high THDi value of 28.27 %. The corresponding harmonic spectrum after compensation using the proposed shunt APF based on a nine-level (NPC) inverter is shown in Fig. 8.



THDi (%) = 28.27%.

Fig. 7 – Source current is (A) spectrum without shunt APF.



THDi (%) = 3.67%.

Fig. 8 – Source current is (A) spectrum with shunt APF based on a nine-level (NPC) inverter.

It is observed that the proposed shunt APF adopting MC-LSPWM modulation strategy can reduce the source current harmonics from 28.27 % to 3.67 %, less than 5 %, and in conformity with 519-IEEE standard norms.

6.2. DYNAMIC PERFORMANCES

To evaluate dynamic responses and test the robustness of the proposed shunt active power filter based on a nine-level (NPC) inverter, a step change in load is introduced between $t_1 = 0.3$ s and $t_2 = 0.4$ s. Figure 9 shows the dc bus voltage. The current and the voltage source waveforms after compensation are simultaneously presented in Fig. 10.

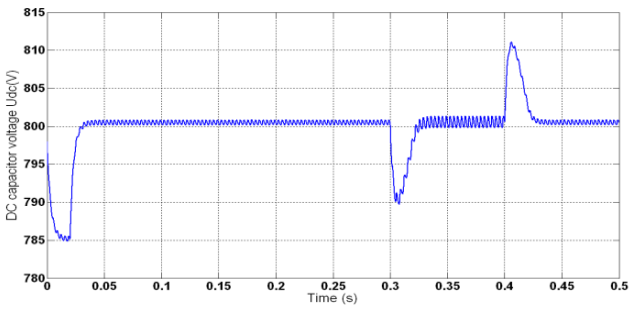


Fig. 9 – Dc voltage with a step change in load.

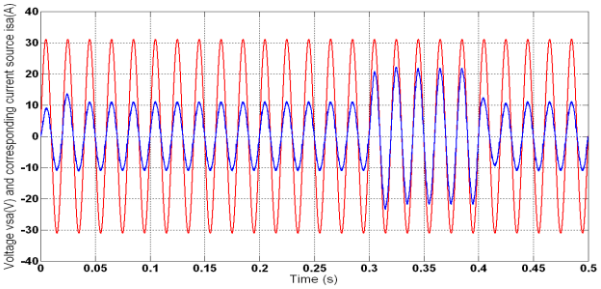


Fig. 10 – Current and voltage source before and after compensation with a load step change.

The dc bus voltage is maintained at a constant value equal to the reference value $U_{dc\text{-}ref}$ = 800 V. The higher number of levels certainly increases the overall performance of the inverter, which is reflected in the results of lower ripple voltage. For the dynamic performances illustrated by Fig. 9, when a step change in load is introduced between t_1 = 0.3 s and t_2 = 0.4 s; the source current is increased. The rise in source current results in increased dc-link voltage with a modest peak equal to 11 V. Figure 10 shows that after shunt APF application, the current source becomes sinusoidal and in phase with the voltage source with improved power factor.

6.3 PERFORMANCES WITH CAPACITIVE NON-LINEAR LOADS

We have performed the following simulations to test the proposed nine-level (NPC) shunt active power filter with capacitive R,C loads. Before t1 = 0.1 s, the source current is distorted due to capacitive loads, as shown in Fig. 11.

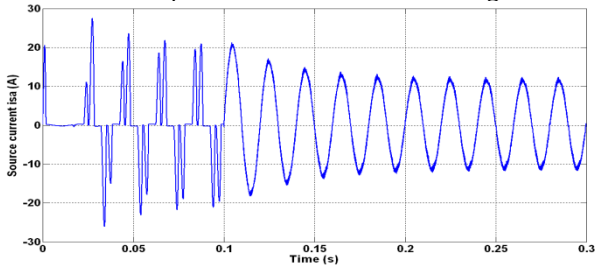


Fig. 11 – Source current before and after compensation

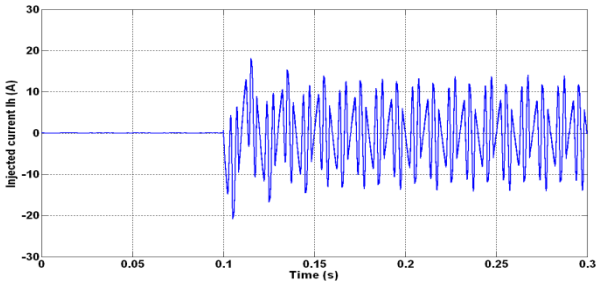


Fig. 12 – Injected current before and after compensation.

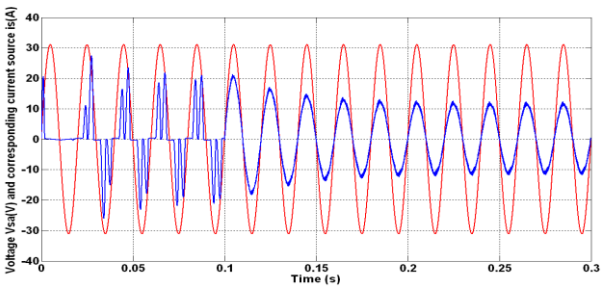


Fig. 13 – Voltage and current source before and after compensation.

To improve the shape of the source current, the shunt APF injects the compensation current given by Fig. 12. After the Shunt APF application at t_2 = 0.1 s shown in Fig. 13, the source current becomes sinusoidal and in phase with the source voltage.

Through visualization Figs. 7–11, we can conclude that the operation of the proposed Shunt APF is successful. Before compensation, the source current is equal to the non-linear load current, highly distorted, and rich in harmonics. After compensation, the THDi is considerably reduced to an acceptable value in conformity with 519 IEEE standard norms (THDi ≤ 5 %).

6.4 COMPARISON WITH OTHER SHUNT APF WITH LESS-LEVEL (NPC) INVERTER

The comparative study between the proposed topology and some previous topologies [14–34] is presented in Table 4. Through this study, we can conclude that the proposed shunt APF system permits the reduction of the THDi to better values than those obtained with similar shunt APF based on three or seven-level (NPC) inverter systems with the same control strategy approaches and in the same simulation conditions. However, using a nine-level (NPC) inverter requires more power components with a complicated control scheme than using less-level (NPC) inverters.

Table 4

Comparison with other shunt APF with less-level (NPC) inverter

Reference	Inverter level	Switch number/phase	THDi (%)	Application
Present study	Nine-level	16	3.67	Shunt APF
Ref. [34]	Seven-level	12	3.79	Shunt APF
Ref. [14]	Three-level	4	4.32	Shunt APF

7. **CONCLUSIONS**

To improve the power quality, novels shunt APF configuration based on a nine-level (NPC) inverter using multicarrier level-shifted modulation control techniques have been proposed in this paper. Several simulations are carried out using MATLAB/Simulink computer simulation with various non-linear loads under different scenarios. The simulation results confirmed the proposed shunt APF's effectiveness in eliminating harmonics, response time, and magnitude of source current during the transient period. The THDi is significantly reduced from 28.27 % to 4.32 % and 3.79 % using three and seven-levels (NPC) shunt APFs. The THDi is decreased to 3.67 % using the proposed system, which conforms with the IEEE-519 standard norms. After compensation, the source current becomes sinusoidal and in phase with the line voltage source with an improved power factor near unity. Through this study, we can conclude that a shunt APF system based on a nine-level (NPC) inverter adopting constant switching frequency multicarrier level shifted pulse width modulation permits the reduction of the THDi to better values than those obtained with less-level voltage (NPC) inverter topologies. This MC-LSPWM technique is efficient for a nine-level inverter, and the proposed Shunt APF system performs well in steady and dynamic states for R-L or R-C non-linear loads. Further research on the considered shunt APF based on a nine-level (NPC) inverter will be focused on the application of advanced control systems to improve the dynamic performances and reduce the THDi.

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