Rev. Roum. Sci. Techn.– Électrotechn. et Énerg.
Vol. **68**, *4*, pp. 325–330, Bucarest, 2023

POWER ENERGY AND POWER AREA PRODUCT SIMULATION ANALYSIS OF MASTER-SLAVE FLIP-FLOP

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Keywords: Master-slave flip-flop; Low power; Digital logic; Power area; Reduced number of transistors.

Flip-flops are the fundamental building blocks of the data path structure. It is a key component of digital circuits and systems. This work offers an exclusive master-slave flip-flop topology by ensuing clocked complementary metal oxide semiconductor (C^2MOS) logic, minimizing the total device count and the count of clocked devices. Reducing the number of clocked devices reduces undesirable transient activity and reduces dynamic power dissipation. C^2MOS logic connects static logic design with clock signal synchronization, resulting in power savings and increased speed. The area reduction is also attained by reducing the total number of devices. The proposed topology has been realized using only sixteen transistors, including six clocked devices, resulting in area compression. Layout-level simulation at 0.12 mm C^2MOS design rule technology is used to investigate the performance. According to an investigation, the proposed topology achieves power savings ranging from 19.77 to 63.75 %, area compaction ranging from 22.03 to 66.30 %, power delay product (PDP) enhancement ranging from 18.56 to 53.91 %, energy-delay product (EDP) enhancement ranging from 5.61 % to 41.39 %, power energy product (PEP) enrichment ranging from 35.63 to 82.82 %, and power area product (PAP) enrichment ranging from 35.19 to 66.30 %.

1. **INTRODUCTION**

A flip-flop is an electronic circuit that stores the logical state of one or more data input signals in response to a clock pulse. It provides information for the design of digital, very large-scale integration (VLSI) systems. It is the most power-consuming component of digital VLSI systems [1,2]. The clock supply network and flip-flop consume 30 % and 60 % of the total chip power [3]. The selection of flip-flop topology is critical in the realization of VLSI integrated circuits such as digital signal processors, microprocessors and controllers, and other high-density integrated circuits (ICs). Factors such as low power, high performance, total device count, number of clocked loads, device heftiness, and the trade-off between power area and energy-delay are commonly considered in an integrated circuit design. Power reduction significantly affects the total power reduction of the clock signal system. As a result, the primary goal of modern digital VLSI system design is to create low-power, high-performance flip-flops with a small footprint.

Pulse-triggered and master-slave flip-flops are found in many modern processors and digital applications. The traditional master-slave flip-flop is constructed with two latches, one with an apparent high value and the other with an apparent low value [4,5]. It can have only one clock nail activated or dual clock nails activated, with harsh edge chattels that are positive time setup and result in excessive propagation delay (D to Q).

Pulse-triggered flip-flops have a shorter propagation delay (D to Q) due to the forgiving edge channel's negative time setup. This can be divided into two categories. Flip-flops are activated by implicit clock pulses [6–9] and explicit clock pulses [10,11]. In recent years, various flip-flop techniques have been designed, such as dual-edge triggered storage element flip-flop (DETSEFF) [12], Power PC [13], flow-through flip-flop with hybrid latch (FLHLFF) [14], flip-flop with control of cross charging scheme (CCFF) [15], semi-dynamic with embedded logic flip-flops (SDELFF) [16], flip flop with conditional data mapping (CODMFF) [17], clock network shared dual edge triggering flip-flop (CNSFF) [18], dual dynamic node flip-flop with hybrid structure (DDNHFF) [19] and D-flip-flop with conditional dynamic pass logic scheme (CPLDDFF) [20] are taken into account with its net count of devices used and count of transistors energized by a clock. However, they are desired for low-power systems due to their power economy.

In a digital organization, the primary source of power dissipation is dynamic switching power dissipation. The ideal expression, which includes the switching transient activity, load capacitance (C_L), supply voltage ($V^2{}_{DD}$), and operating frequency, can be used to evaluate it (F_{CLK}),

$$P_{switching} = \alpha \cdot C_L \cdot V^2{}_{DD} \cdot F_{CLK} . \quad (1)$$

Regarding these factors, several approaches are available to reduce power consumption, which are listed below [2]:

- minimizing the number of clocked devices;
- minimizing the total device counts;
- reducing the switching activity;
- curtailing short current power;
- minimizing static and leakage current;
- multiple voltage drain to drain (VDD) scheme;
- path splitting scheme.

As power density develops alarmingly, Khan I.A. [21] introduced a semi-dynamic master-slave single-edge triggered flip-flop design. Power management is becoming an increasingly important issue for every level of design. A performance analysis of the different master-slave flip flops that have been reported is presented by Chopra U. [22], along with a comparison of their characteristics, including power, area, delay setup time, and hold time. Furthermore, Wu H. et al. [23] suggested a high-speed quaternary D flip-flop that relies on multiple current values. Chowdary G.R. [24] designed a D-flip-flop using possible technology nodes for all synchronized circuits.

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DOI: 10.59277/RRST-EE.2023.68.4.19

Yuan H. [26] presented a flip-flop with a sensory amplifier that operates quickly and with little power. The proposed SAFF can also run at low voltage due to MTCMOS optimization. For low supply voltage (VDD) functioning, Jeong H. [25] presented a sense amplifier-based flip-flop with transition completion detection (SAFF-TCD). Shah O.A. [28] addressed the speed decreases and power consumption at higher data activities in previous approaches by proposing a better sense amplifier-based flip-flop design for low-power and high-data activity circuits. A low overhead warning flip-float for timer leak monitoring was proposed by Cantoro R. et al. [29]. Unlike the traditional worst-case architecture under typical conditions, it has a master-slave FF, a delay buffer, and a warning generator. Several related studies have been conducted; however, reducing energy delay in flip-flops is still the major issue in VLSI. In this research, master-slave pulse-trigger D-flip-flop (MS-PTDFF) is built with clocked CMOS (C^2MOS) logic, and regeneration loops have been introduced to reduce the power savings, increased speed, and a reduction in the number of devices.

The rest of the article is structured as follows. In section 2, the literature review is fully explained. Section 3 describes the proposed C^2MOS approach. Section 4 contains the performance and comparative analysis. Section 5 discusses the conclusion.

3. PROPOSED MASTER SLAVE PULSE TRIGGERING D FLIP FLOP (MS-PTDFF)

This section proposes a novel topology for pulse-triggering D-flip-flops in a master-slave environment. This master-slave pulse-trigger D-flip-flop (MS-PTDFF) is built with clocked CMOS (C^2MOS) logic and regeneration loops. It uses the master section to sample the D input precisely at the leading nail of the clock (CLK = HIGH) and transfers the data to the output node at the trailing nail of the clock (CLK = LOW).

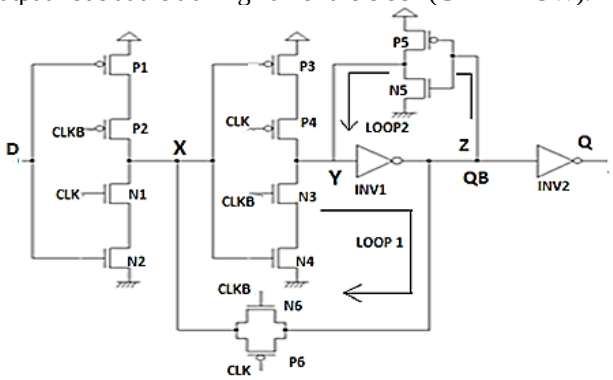

Fig. 1 – Master-slave pulse-triggering D-flip-flop (MS-PTDFF).

The proposed MS-PTDFF is realized in four stages, with 16 transistors, including 6 clocked devices, as depicted in Figure 1. The first two stages are latching stages with C^2MOS latches, and the later stages are inverter stages with inverter 1 (INV1) and inverter 2 (INV2). The flip-flop's heart is a C^2MOS latch composed of four devices: P1, P2, N1, and N2. The transistors P1 and N2 capture the input D, and the pair of complementary clock signals is implicitly given to the P2 and N1 transistors. The C^2MOS latch will be an inverter if the clock input is HIGH (CLK = 1). Therefore, the input data D will be inverted and appear as the first stage output at node x. In this first stage, the C^2MOS latch will act as master and be accountable for catching the input node data.

The C^2MOS latch is duplicated and placed next to the first latching stage using P3, P4, N3, and N4 transistors. The transistors P4 and N3 will be enabled by a clock pair that does not overlap with the clock pair used in the first latching stage. While the clock input is low (CLK = 0), the second latching stage acts as an inverter, resulting in the inverted first-stage output at node Y. This duplicated second-stage C^2MOS latch will function as a slave, responsible for data transport to the output node. An inverter, INV1, is a stage 3 element next to the slave latch. The second stage output feeds inverter 1, and the complemented value appears at node Z. The signal visible at Z is the complemented output QB. Inverter INV2 is located directly next to INV1 and is the fourth stage element. It completes the signal QB and yields the expected output Q.

The clocked transmission gate is between points X and Z, forming the regeneration loop L1. The C^2MOS inverter connects nodes Y and Z, activating the regeneration loop L2. Two inversions take part in the forward via (critical path) in this suggested topology, and an inverter completes loop L2. Loop L1 is completed by maintaining a timed switch (transmission gate) in the feedback path. To achieve the static functionality of the circuit, a few loops act in a regenerative manner in the master-slave structure. In this anticipated topology, the output node never encounters the floating node issue and is always driven. Thus, the static operation is ensured in the offered flip-flop realization.

3.1. FUNCTIONALITY OF THE PROPOSED CIRCUIT TOPOLOGY IS ELABORATED AS FOLLOWS

In the master-slave realization, a pair of latching stages are coupled in a back-to-back master-slave pattern with opposite phase clocks. The input side of the flip-flop is dealt with by the first of two latching stages, known as the master, while the output port is dealt with by the second, known as the slave. An ad edge is not triggered 100 % of the time. When the clock's positive edge arrives at the master stage, it enters evaluation mode and samples the input data D. At the same time, the later slave stage enters hold mode, and its output becomes high impedance. When the clock's negative edge arrives, the master enters holding mode and transfers data to the slave stage. Meanwhile, the slave stage transitions to an evaluation phase, capturing data from the master and transferring it to the output net.

In the suggested master-slave configuration, the devices NI and P2 turn on simultaneously as the input data is asserted to HIGH (D = 1), and the leading nail of the clock signal is seen (CLK = 1 and CLKB = 0). Because D = 1, the device P1 turns off, and the device N2 turns on. In this state, the master latch acts as an inverter, evaluating the inverted data value (D = 0) and transferring it to node X (X = 0). While this happens, the slave-stage transistors P4 and N3 go into hold mode and turn off. In this case, the value of node Y becomes high impedance, separating the output node from the input node. The output Q retains its previous state.

As the input data remains HIGH (D = 1) and the clock signal's trailing nail appears (CLK = 0 and CLB = 1), the devices NI and P2 turn off. The transistors N2 and P1 are turned on. In this case, the master section enters hold mode and does not sample the input data. Meanwhile, because CLK = 0 and CLKB = 1, both P4 and N3 devices turn on, act as inverters, evaluate the signal X = 0, and transfer its inverted value to node Y = 1. The third-stage inverter INV1 inverts the value Y = 1 and produces the result Z = 0. The complement of the anticipated output is considered to be the output at node z, or QB.

In the fourth section, an inverter INV2 inverts the value of Z = 0, resulting in Q = 1. The regenerative loops L1 via CMOS

inverter and L2 via transmission gate ensure the flip-flop topology's static functionality. Only after one full clock pulse duration arrives does the master-slave flip-flop finish its action. The lengthy operational cycle is categorized into two phases.

PHASE 1:

If D = 1, CLK = 1(POSITIVE CLOCK EDGE ARRIVAL) & CLKB = 0 then

N1 = OFF, P2 = OFF, first master latch (evaluation mode) = inverter, N3 = OFF, X = 0, P4 = OFF Hold mode is represented by the second slave latch. Y denotes a high impedance value, Z denotes a high impedance value, and Q denotes the previous state.

PHASE II:

For same D = 1, while CLK = 0 (NEGATIVE CLOCK EDGE ARRIVAL) & CLKB =1 ,

N1 = OFF, P2 = OFF, first master latch (non-evaluation mode), X = previous state (X = 0).

N3 = ON, P4 = ON, 2nd slave latch (evaluation mode) = inverter Y = 1, Z = QB = 0 and Q = 1 (HIGH) In other words, Q = D (input = output).

In this proposed MS-PDTFF, input data D enters the master stage at the leading nail of the clock pulse, and output is obtained at the end of the slave stage during the trailing nail of the clock pulse. As a result, the master-slave flip-flop completes its operation at the end of one full clock pulse cycle. As a result, it is known as a pulse-triggering flip-flop. The C^2MOS latch, which serves as the flip-core flop's fragment, eliminates the clock overlapping issue. Because the master and slave latches are enabled by opposing phase commentary clock pairs, it eliminates the possibility of clock pulses overlapping. C^2MOS logic causes the rise and fall times to be if they are fast. It avoids the potential error that can occur between pull-down and pull-up networks. This results in lower static power and topography density [23,24].

The proposed flip-flop can be realized with only sixteen transistors by successfully reducing the number of devices, making the proposed design area efficient. Furthermore, by minimizing the number of clocked devices, the proposed design employs only six counts of clocked devices out of a total of sixteen devices. This technique reduces the unsolicited switching activity of transistors, resulting in a decrease in dynamic power dissipation.

The incorporation of back-to-back regeneration loops ensures the circuit's static functionality. The output node is always driven and is never a floating-point node. As a result, the floating node dispute is eliminated in this proposed construction. All of these subsequent approaches, such as C^2MOS logic, reducing total device count, reducing clocked load count, using regeneration loops, and eliminating the floating node problem, make the MS-PTDFF design area and power efficient.

4. RESULTS AND DISCUSSION

The proposed design is schematized in DSCH and simulated at the layout level using MICROWIND EDA. The clock signal's maximum switching transient factor in contemporary digital CMOS logic design is approximately 1. In this proposed work, those devices that occur in the latching stages and feedback paths activated by the CLK signal are increased to 100 % transient activity devices.

The traditional optimization parameters, including power & energy product (PEP), energy & delay product (EDP), and power & delay product (PDP), are evaluated for the proposed circuit design. PDP (Power + Delay) gives delay and power equal weights. Together, delay and power are equally optimized by PDP. EDP (energy + delay) prioritizes design performance concerning operating speed. EDP (power, delay, and delay) evaluates design quality. If power is the foremost concern, then PDP and EDP metrics cannot provide the right solutions. The circuit must be optimized for the PEP (power * power * delay) metric. PEP adds rank to power compared to delay and yields an efficient power solution compared to the previous two metrics [25].

The new-fangled optimization metric named power area product (PAP) is considered for this work. PAP is calculated as power * area. It gives equal geometric weight to both power and area. This proposed work is optimized for both power and area. As a result, the proper metric PAP is estimated for this work to test both power efficiency and area compaction.

The proposed MS-PTDFF consumes one full clock cycle to sample the input data and transfer it to the output net. Its functionality is tested for the following conditions:

OPERATION 1: for D = HIGH

Phase I: D = 1, CLK = 1, CLKB = 0, X = 0, Y = high impedance (HIM), QB= high impedance and Q = previous state value. (Master in evaluation mode, Slave in holding mode)

Phase II: D = 1, CLK = 0, CLKB = 1, X= high impedance, Y= 1, QB= 0 and Q=1. (Master in holding mode, Slave in evaluation mode)

OPERATION 2: for D = LOW

Phase I: D = 0, CLK = 1, CLKB = 0, X = 1, Y= high impedance, QB= high impedance and Q = previous state value. (Master in evaluation mode, Slave in holing mode)

Phase II: D=0, CLK =0, CLKB =1, X= high impedance, Y= 0, QB= 1 and Q=0. (Master in holding mode, Slave in evaluation mode)

The schematized proposed flip-flop circuit on the DSCH schematic editor is reported. The operations mentioned above of the newly proposed design are evaluated under varying configurations of D-data input and CLK and CLKB indications, as shown in Figs. 2a, 2b, 3a, 3b, 4a, 4b, respectively. Figures 6 and 7 demonstrate the output waves of MS-PTDFF, power utilization, and physical layout.

4.1. PERFORMANCE METRICS

The performance matrices such as overall count of devices used, count of loads energized by a clock, physical area occupation (A), total power utilization (P), propagation delay time (D-Q), and metrics such as PDP, EDP, PEP, and PAP for an optimization are manipulated to evaluate the prominence and potential of the anticipated topology with the prior technique.

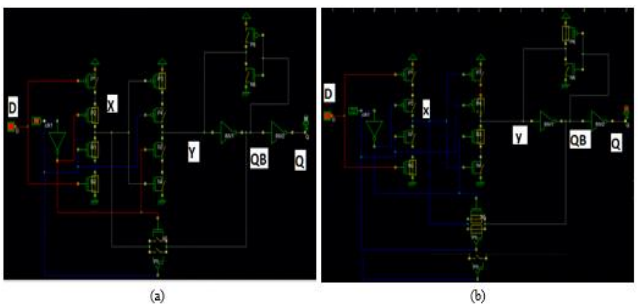

Fig. 2 – a) Functionality 1: phase I: D = HIGH (1);
b) phase II: D = HIGH (1).

CLK = leading edge (1), CLKB = 0, X = 0, Y = HIM, QB = HIM, and Q = previous state value (master in evaluation mode, Slave in holing mode). CLK = trailing edge (0), CLKB =1, X = HIM, Y = 1, QB = 0, and Q=1 (master in holding mode, slave in evaluation mode).

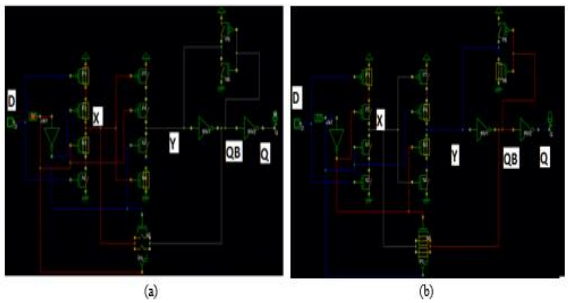

Fig. 3 – a) Functionality 2: Phase I: D = LOW (0); b) Phase II: D = LOW (0).

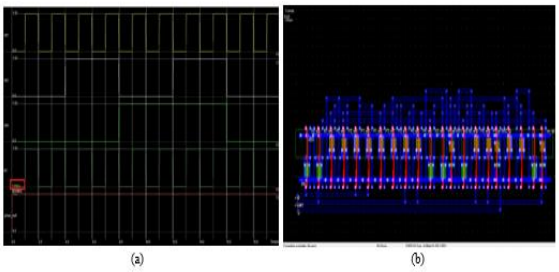

Fig. 4 – a) Desired output waveform of proposed MS-PTDFF with power utilization of 5.945 µW; b) layout of proposed MS-PTDFF with area of 252 µm^2.

CLK = leading edge (1), CLKB = 0, X = 1, Y= HIM, QB = HIM\and Q = previous state value (master in evaluation mode, slave in holing mode) CLK = Trailing edge (0), CLKB = 1, X = HIM, Y = 0, QB = HIGH (1) and Q = 0 (master in holding mode, slave in evaluation mode).

Table 1

Comparison of performance metrics for proposed with existing flipflop

Sequential circuits	Performance Metrices					
	Total number of devices	Number of clocked devices	Activating type	Layout area [µm^2]	Propagation delay [ps]	Total power [µW]
DETSEFF	30	16	Dual edge	545	163	16.39
POWER PC	22	8	Single edge	428	175	13.423
FLHLFF	20	10	Single edge	313	159	12.275
CCCFF	21	4	Single edge	339	162	11.122
SDELFF	23	7	Single edge	263	156	11.027
CODMFF	22	7	Singe edge	428	177	10.276
DDNHFF	18	6	Single edge	299	165	9.724
CNSFF	23	8	Dual edge	423	178	8.346
DPL-DETFFF	18	4	Dual edge	312	282	7.410
Proposed MS-PTDFF	16	6	Pulse Triggering	252	206	5.945

Table 2

Comparison of optimization metrics for proposed with existing flipflops

Sequential circuits	Optimization Metrices			
	PDP (fj)	EDP (10^{-24})	PEP (10^{-20})	PAP [µm^2] * [µw]
DETSEFF	2.65	0.430	4.355	8954.4
POWER PC	2.36	0.414	3.171	5758.896
FLHLFF	1.93	0.304	2.381	3830.112
CCCFF	1.81	0.294	1.134	3759.574
SDELFF	1.72	0.267	1.897	2712.888
CODMFF	1.83	0.326	1.879	4408.833
DDNHFF	1.61	0.267	1.130	2907.775
CNSFF	1.50	0.269	1.264	3539.128
DPL-DETFFF	2.089	0.589	1.548	2311.92
Proposed MS-PTDFF	1.224	0.252	0.728	1498.14

Considering the performance and optimization metrics, Tables 1 and 2 validate the results of the proposed and existing MS-PTDFF designs, respectively. Pie and bar graphs are provided to evaluate the performance and optimization metrics quickly.

In comparison to existing designs, this is the lowest total number of devices used. With the exception of CCCFF and DPL-DETFF, MS-PTDFF reduces clock transistor costs by 14.28 % to 62.5 % and saves 11.11 % to 46.66 % of the total count of devices when compared to existing elements. The MS-PTDFF has six clock-enabled transistors, which results in 33.33 % more clocked load counts than the CCCFF and DPL-DETFF.

4.2. COMPARATIVE ANALYSIS

Comparing the proposed MS-PTDFF to existing flip-flop designs, it takes up the least space on the layout and achieves a layout area efficiency of 4.54 % to 53.84 %. By reducing the total number of devices, less space is occupied, which increases the suggested design's efficiency in terms of space use.

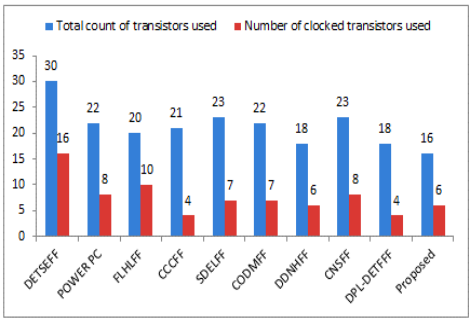

Fig. 5 – Overall transistors count and count of clocked devices.

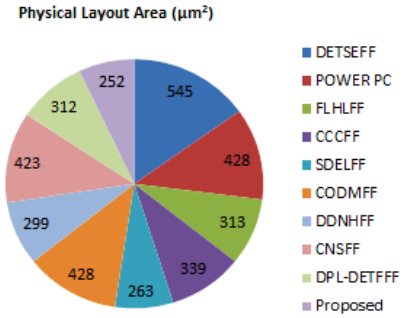

Fig. 6 – Contrast of physical area occupation.

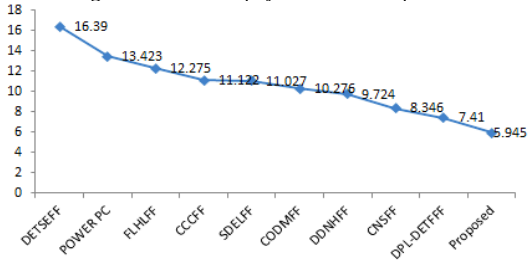

Fig. 7 – Contrast of total power utilization.

The MS-PTDFF topology adds 206 PS to the propagation delay (D-Q). The latency is reduced by 26.95 % when compared to the current DPL-DETFF. The proposed building would take longer than necessary if it were to match existing designs. Even though master-slave flip-flops are power-efficient, choosing between them and the suggested flip-flop for high-performance applications is difficult due to their substantial propagation delays.

Regarding total power utilization, the suggested MS-PTDFF uses a net power of 5.945 compared to all prior flip-flops in comparison to Table 1; the suggested architecture achieves power efficiency ranging from 19.77 % to 65.34 %.

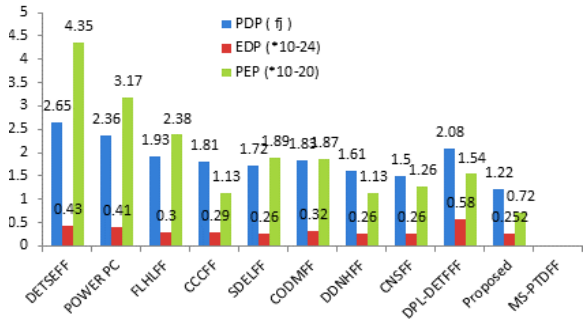

Fig. 8 – Contrast PEP, EDP, and PDP.

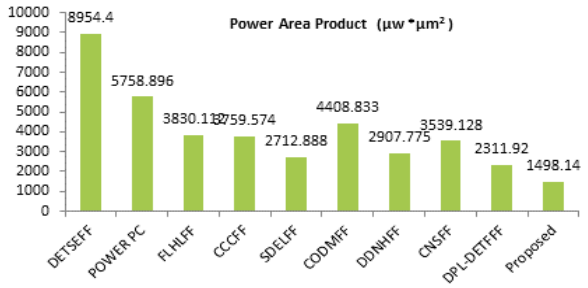

Fig. 9 – Contrast of power & area product (PAP).

This proposed architecture is power efficient using C²MOS circuitry and reduced timed loads. The figures in Table 2 show that the suggested MS-PTDFF has a PDP value of 1.224 fj and has improved from 18.56 % to 53.91 % compared to the currently used designs. Following the EDP point, the MS-PTDFF circuit obtains a roughly 0.252 x 1024 value. Compared to all currently used flip-flop designs, the MS-PTDFF design's EDP cost has increased from 5.61% to 41.39 %.

5. CONCLUSIONS

This work presents a new topology for D-flip-flops that uses less energy and occupies less space physically in a master-slave system. The proposed architecture uses only sixteen transistors, including six timed devices. The C²MOS logic and fewer clock devices reduce overall power consumption. Placing the core C²MOS latches in the vital data path and eliminating the unwanted transistor switching activity makes a rise in power efficiency of 19.77 % to 65.34 % possible. This topology ensures that an output node Q is always powered by the forward connection path, excluding the floating node problem. Furthermore, the design's static operation is guaranteed with a delay penalty due to the back-to-back retention loops. The proposed topology minimizes power as well as area. The optimization metric PAP is used to assess the significance and potential of the proposed topology. The overall PAP of the proposed method is 34.91 % and 83.26 % improved in existing DPL-DETFFF and DETSEFF techniques, respectively. Overall, the C²MOS logic makes the proposed MS-PTDFF more power efficient by reducing the total number of clocked devices and improving loop retention. and are efficient. According to the evaluation results, the proposed master-slave D flip-flop may be effective for low-power and low-area systems.

ACKNOWLEDGMENTS

With deep gratitude, the author would like to thank the supervisor for his guidance and constant support during this research.

Received on 1 February 2023

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