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WIDE BOOST RATIO IN QUASI-IMPEDANCE NETWORK CONVERTER USING SWITCH VOLTAGE SPIKE REDUCTION TECHNIQUE

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Keywords: Modified quasi-impedance source converter; Conventional quasi-impedance source converter; Switched capacitor; Inductance alone; Embedded; Voltage ripple, Voltage stress; Voltage gain.

High-step-up converters are widely used for solar power applications. In that, impedance source converters are mostly preferred as it has a special feature of high gain at a low-duty cycle. However, the traditional impedance source converters have limited duty ratio operation and high stress across the network and the device. Thus, this paper presents a new type of quasi-impedance source dc-dc converter. The proposed converter has a large boost ratio operation using a switch voltage spike reduction technique. This reduces the stress across the network as well as across the device. The performance of the proposed topology has been investigated against several types of quasi-impedance source converters such as a switched capacitor, inductance alone, embedded, and conventional quasi-impedance source converter. The results clearly show that the projected modified quasi-impedance source converter topology has a high efficiency of 92 %. The modes of operation and comparative study of the modified topology are presented. A 60 W laboratory setup is developed to investigate the performance of the suggested converter, and the simulation results are verified experimentally.

1. INTRODUCTION

Nowadays, renewable energy sources have been used for many applications due to their pollution-free feature and the shortage of fossil fuels [1]. However, the output voltage from such sources is low, and thus, it requires a high gain step-up dc-dc converter. Also, in solar power generation, the output power varies due to partially shaded conditions, and thus, dc-dc converters are essential to provide steady and controlled output power [2]. The various step-up converters have been reviewed in the literature [3]. They are categorized as isolated, non-isolated converters, and unidirectional and bidirectional converters. The most widely employed converter is the boost converter, which has a high boost factor when the duty cycle approaches 1. But, practically, the presence of parasitic elements limits the duty cycle of the boost converter. Hence, the application of boost converter is limited [4]. To increase the boost factor, the traditional boost converters are cascaded [5]. However, the controller implementation is complicated, increasing the converter size. In [6], the interleaved converter has been explained, which reduces the output voltage and current ripple and attains a high voltage conversion ratio. But, the number of inductors required increases the interleaved topology's size. The integrated cascaded boost converter has been reviewed in [7] to reduce the switch count.

Further, to reduce the passive elements count, coupled inductors replace the inductors [8]. A high voltage gain can be attained in such a converter, but it requires an additional auxiliary circuit to mitigate the problem associated with the leakage inductance. Also, switched inductors and switched capacitor configurations have been discussed in [9]. The voltage conversion ratio can be improved by adding a voltage multiplier cell to the boost converter [10]. However, all these converters only satisfy some of the requirements needed for high-power applications and probably increase the cost and size of the converter.

Thus, the impedance source converter (ZSC) concept emerged, which can be applied to all power conversion topologies. Since ZSC has efficient power conversion for a broader range, it can be used in industrial applications such as EVs, solar PV systems, distributed generation, and energy storage systems [11]. The Z-source converter consists of an LDC unit (inductors, capacitor, and diode) placed between the input (in series with the input) and load. The inductors and capacitors in the LDC unit are connected in an X shape [12]. By properly controlling shoot-through, the ZSC can accomplish both boost and buck operation. Though ZSC has been widely used, it has the drawback of discontinuous source current due to a diode in series with the input. This evolved in the development of a quasi-impedance source converter (QZSC). It has the same merits as ZSC and has special features such as continuous source current, reduced stress across the network, and improved efficiency [13]. A high voltage conversion ratio is achieved by replacing the input inductor with an impedance network in the traditional boost converter [14]. All other techniques, such as boost-buck operation, cascading, interleaved concept, switched inductor and switched capacitor, can also be done with the QZSC. Many topologies of QZSC have been reviewed in the literature [15–17]. Many impedance network topologies are developed to establish an efficient power conversion for a wide range of input and load values. The converters include trans-Z-source [18], T-source [19], Y-source [20], A-source [21], Γ-source [22], TZ-source [23], resonant impedance source converter [24], and converter with magnetic coupling [25]. Each has its own merits and demerits. The conventional QZSC in [26] has a high voltage conversion ratio and reduced output voltage ripple, but the stress across the network is still high. With a switched capacitor network [27], the stress may be reduced, but the requirement of passive elements is increased and has low efficiency. The embedded converter proposed in [28] may increase the efficiency, but still, the performance has to be improved. The converter in [29] has only the inductor eliminating the capacitor in the network; thus, it is called inductance alone QZSC. This reduces the output voltage ripple and stress across the network, but it possesses low efficiency. Hence, all the converters proposed in [26–29] do not satisfy the essential requirements of an efficient dc-dc converter for EV battery charging applications.

Thus, a new converter based on conventional QZSC has been discussed in this paper. The presented converter replaces one of the capacitors with a diode in the

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impedance network. Due to this, the stress across the network and the device is lowered as it reduces the inrush current and voltage ringing for a wide range of voltage conversion ratios. This results in a linear voltage gain profile for the proposed converter.

The modified QZSC has a high voltage conversion ratio, high efficiency, reduced output voltage ripple, and reduced network and switch stress. The operation of QZSC in both continuous current mode (CCM) and discontinuous current mode (DCM) depends on the connection of the LDC unit. Compared with the CCM configuration, the DCM configuration of QZSC is preferred since the network capacitor voltage stress is much reduced with this configuration. Though the quasi Z-source converter is in DCM configuration, it operates in CCM mode until it reaches the boundary conditions. The boundary condition for CCM and DCM of QZSC is given in equation (1) [25]. Whenever the load resistor R_L is less than the R_{Lmax} depicted in equation (1), QZSC operates in CCM. But, if the load resistor R_L is greater than the R_{Lmax}, QZSC operates in DCM.

$$R_{Lmax} \leq \frac{2Lf_s}{d\,(1-d)(1-2d)}, \quad (1)$$

where, L = inductance, f_s = switching frequency, and d = duty ratio.

Hence, the proposed converter in DCM configuration is chosen for analysis and implementation. For comparative analysis, the existing topologies such as conventional QZSC, switched capacitor QZSC, embedded QZSC, and inductance alone QZSC are taken. The performance of the suggested modified converter for all the duty cycle values is computed and compared with the existing topologies. The parameters accounted for analysis are voltage gain (G), output voltage ripple (ΔV_o), network capacitor voltage stress (V_{cs}), network diode voltage stress (V_{ds}), switch voltage stress (V_{ss}), efficiency (Π), and the number of passive components.

The paper's organization is as follows: The different topologies of quasi-Z-source converters have been discussed in section 2. The design and the simulation results of the modified QZSC are presented in section 3. A comparative analysis of all the converters is depicted in section 4. Section 5 and section 6 deal with the hardware result and its discussion**.**

2. QUASI IMPEDANCE-SOURCE CONVERTER TOPOLOGIES

This section reviews the converter topologies such as conventional QZSC, switched capacitor QZSC, embedded QZSC, inductance alone QZSC, and proposed modified converter taken for analysis. The operation and circuit diagram of each converter has been explained in this section.

2.1 CONVENTIONAL QZSC

The schematic representation of a conventional quasi-Z-source converter is presented in Fig. 1 [26]. The inductors L1 and L2, capacitors C1 and C2, and diode D constitute the impedance network. The output diode, capacitor, and load resistors are denoted as D0, C0, and R. The operation of conventional QZSC is divided into two modes. In mode 1, the switch S is in conduction, and diodes D and D0 are turned off; the input voltage source Vin and capacitors C1 and C2 charge the inductors L1 and L2.

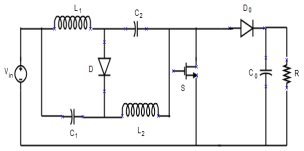


Fig. 1 – Conventional QZSC.

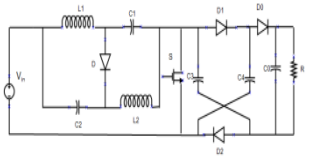


Fig. 2 – Switched Capacitor QZSC.

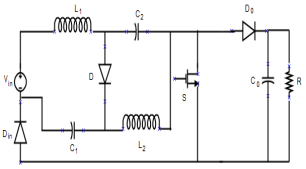


Fig. 3 – Embedded QZSC.

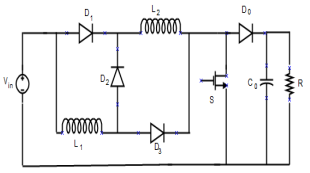


Fig. 4 – Inductance alone QZSC.

The operation of conventional QZSC is divided into two modes. In mode 1, the switch S is in conduction, and diodes D and D0 are turned off; the input voltage source Vin and capacitors C1 and C2 charge the inductors L1 and L2. Thus, the inductor current increases linearly. In mode 2, the diodes D and D0 get turned on, and switch S is turned off; the inductors discharge the current to load R through capacitors. Hence, the inductor current decreases linearly.

2.2 SWITCHED CAPACITOR QZSC

The pictorial representation of the switched capacitor QZSC is presented in Fig. 2. The capacitors C_3 and C_4 and diode D_1 and D_2 constitute the switched capacitor network [27].

When switch S turns on, the capacitors C_3, C_4, and C_0 discharge through the load simultaneously, and the inductors L_1 and L_2 get charged by the capacitors C_1 and C_2 and the input voltage source. When the switch is in the off state, the input voltage source delivers the power to the load through the impedance network and switched capacitor network, increasing the converter's boost factor. In this case, the network capacitors are charged by the network inductors.

2.3 EMBEDDED QZSC

In embedded QZSC, the source voltage is embedded with the impedance network, as shown in Fig.3, and the input diode D_{in} is in series with the source [28].

The construction and operation are similar to the ZSC, but the only difference is with ZSC, the source current is chopped because of the presence of an input diode. This embedded topology can overcome this, where the source current is filtered without any auxiliary circuit. The voltage conversion ratio of the embedded QZSC and conventional QZSC are identical.

2.4 INDUCTANCE ALONE QZSC

In inductance alone, QZSC presented in Fig. 4, the capacitor requirement is eliminated. Only the inductors and diodes are used in the network to couple between the input and output ports [29]. Because of the elimination of capacitors in the network, the stress across the network and the device can be eliminated. With this QZSC, the voltage gain can be improved, reducing the effect of start-up currents.

2.5 MODIFIED QZSC

The suggested modified QZSC is presented in Fig. 5. The inductors (L_1, L_2), capacitor (C_1), and diodes (D, D_1) constitute the impedance network. The capacitor C_2 in the conventional QZSC is replaced by diode D_1 in the modified QZSC.

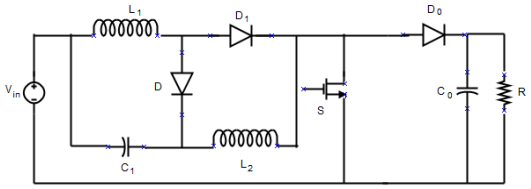
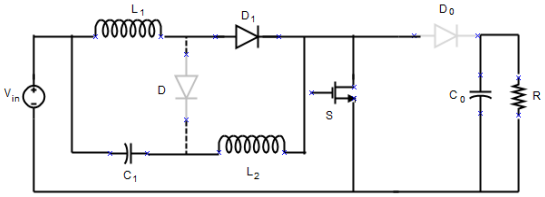
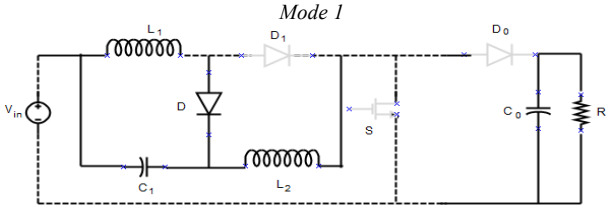


Fig. 5 – A modified quasi-impedance network converter.

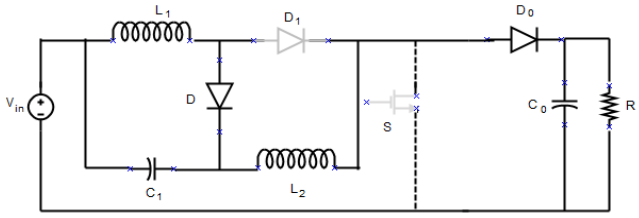
The working principle of the modified converter is explained below, and its pictorial representation is depicted in Fig. 6. In Fig. 7, the relevant waveforms are illustrated.



Mode 1



Mode 2



Mode 3

Fig.6 – Operation of the modified converter

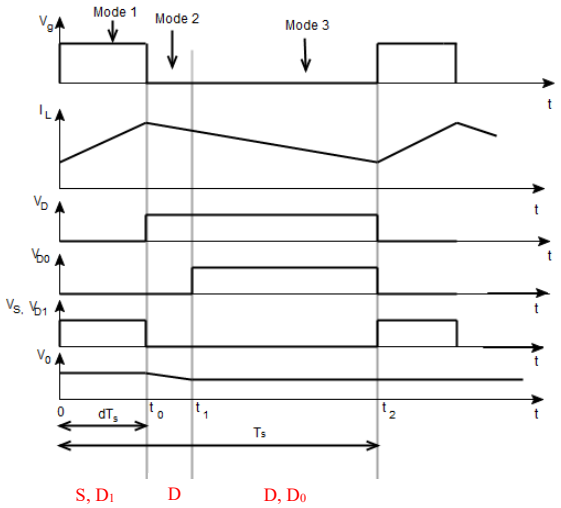


Fig. 7 – Waveforms of the modified converter.

Mode 1 [0 ~ t_0]: in this mode, the switch S and the diode D_1 are in conduction, whereas the diodes D and D_0 are turned off due to reverse bias conditions. During this mode, the capacitor C_1 and source voltage charge the inductors (L_1 and L_2), and thus, the inductor current increases linearly, as shown in Fig. 7.

Mode 2 [t_0 ~ t_1]: *i*n mode 2, switch S and diode D_1 are in off condition, and the inductor current charges the capacitor C_1; thus, it decreases linearly, as depicted in Fig. 7. Due to this, the diode D gets turned on but, the diode D_0 remains in off state as the output voltage is greater than the switch voltage. This makes the impedance network isolated from both the input and output sides. When the output voltage becomes less than the switch voltage, the diode D_0 gets turned on, and mode 2 ends.

Mode 3 [t_1 ~ t_2]: in Mode 3, *S*witch S remains turned off, and the diodes D and D_0 are on condition. The inductor current still decreases as it charges the capacitor C_1, as depicted in Fig. 7. Now, the source powers the load through the impedance network, and simultaneously, the capacitor C_1 gets charged.

3. DESIGN AND SIMULATION RESULTS OF MODIFIED QZSC

The recommended modified topology is modeled and simulated in MATLAB/Simulink. The simulation parameters are calculated using the equations described in [26]. The voltage waveform and stress waveform of modified QZSC are depicted in Figs. 8, 9. The expression of the inductor and capacitor is given below, assuming that the converter operates in continuous current mode (CCM), and all the parameters are under ideal conditions. The inductor is,

$$L = \frac{2d\,(1-2d)V_{in}}{(1-2d)\Delta I_L f_s}, \tag{2}$$

where, ΔI_L= 10 to 30 % of I_L, I_L = inductor current, f_s= switching frequency, and d = duty ratio.

The capacitor is found by:

$$C = \frac{I_L d}{\Delta V_c f_s}, \tag{3}$$

where, ΔV_c = 1 to 5 % of V_o, and V_o = output voltage.

The mathematical expression for stress across the capacitor and switch is described below:

$$V_s = \frac{1}{1-2d} V_{in}, \tag{4}$$

$$V_c = \frac{d}{1-2d} V_{in}. \tag{5}$$

Based on the expression described in eq. (2), (3), the parameter values are evaluated and listed in Table 1.

Table 1

Simulation Parameters

Parameters	Rating
Supply voltage (dc)	40 V
Output voltage	52 V
Duty Ratio	0.15
Inductor (L)	147 µH
Capacitor (C)	413 µF
Load resistor (R)	25 Ω
Switching frequency	25 kHz

The source voltage of 40 V is boosted to 52 V, as depicted in Fig. 8 for the duty ratio of 0.15; thus, the voltage gain is 1.3. It is also seen that the output voltage ripple is 0.014 V. From the simulation results, the capacitor voltage stress is about 5.8 V, and the switch voltage stress is about 52.9 V, which validates the theoretical values depicted in eq. (4), (5).

Thus, the voltage stress across the network diode (V_{ds}) is 0.99 ($\frac{V_d}{V_i} = \frac{39.98}{40}$), the network capacitor voltage stress (V_{cs}) is 0.14 ($\frac{V_c}{V_i} = \frac{5.81}{40}$), and the voltage stress across the device (V_{ss}) is 1.32 ($\frac{V_s}{V_i} = \frac{52.9}{40}$) as depicted in Fig. 9.

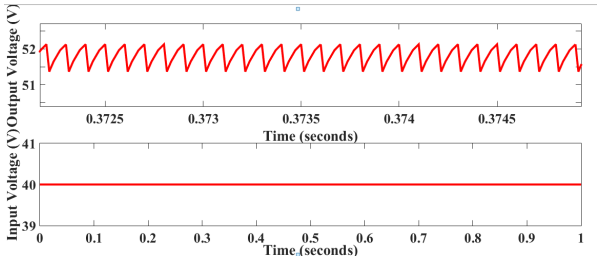


Fig. 8 – Input and output voltage of modified QZSC.

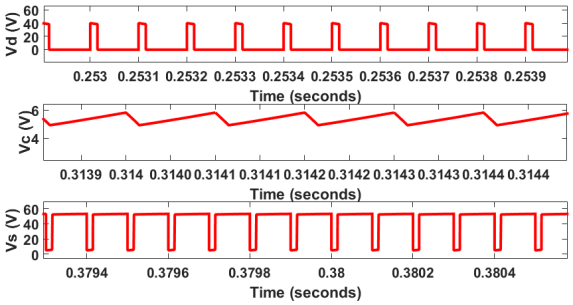


Fig. 9 – Stress waveform of modified QZSC.

4. COMPARISON OF PROPOSED CONVERTER WITH OTHER CONVERTERS

The keywords section is left-aligned, left, and right The parameters taken for analysis are voltage gain ($G = \frac{Output\ Voltage\ (V_0)}{Input\ Volage\ (V_{in})}$), output voltage ripple ($\Delta Vo = \frac{V_{0max} - V_{0min}}{V_{0avg}}$), network capacitor voltage stress ($V_{cs} = \frac{Voltage\ across\ the\ capacitor\ V_c}{Supply\ voltage\ V_i}$), network diode voltage stress ($V_{ds} = \frac{Voltage\ across\ the\ diode\ V_d}{Source\ voltage\ V_i}$), switch voltage stress ($V_{ss} = \frac{Voltage\ across\ the\ switch\ V_s}{Supply\ voltage\ V_i}$), efficiency ($\eta = \frac{P_{out}}{P_{out} + P_{loss}}$), and the number of passive components [30]. The analysis is carried out for all the five topologies described in section 2 for different duty ratios. The pictorial representation of the analysis of all the converters is depicted in Fig. 10 to 15.

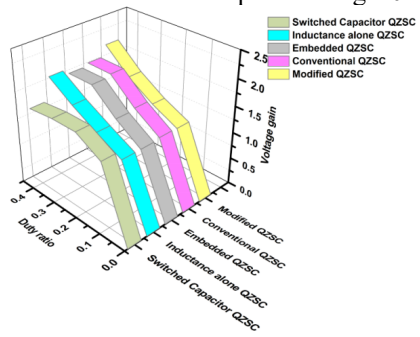


Fig. 10 – Voltage gain.

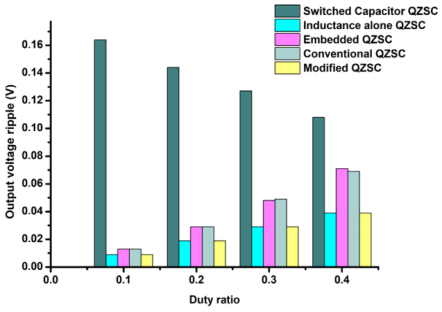


Fig. 11 – Output voltage ripple.

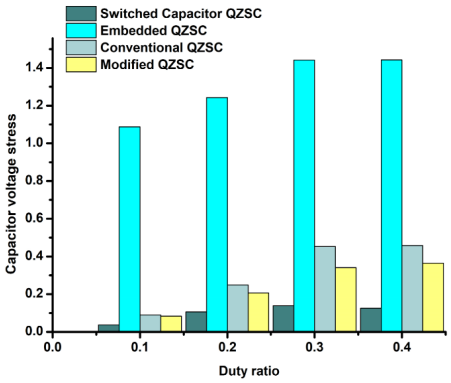


Fig. 12 – Capacitor voltage Stress.

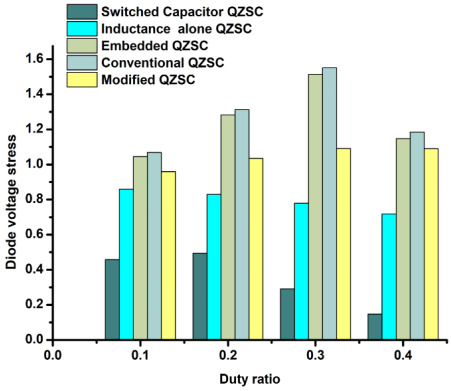


Fig.13 – Network diode voltage stress.

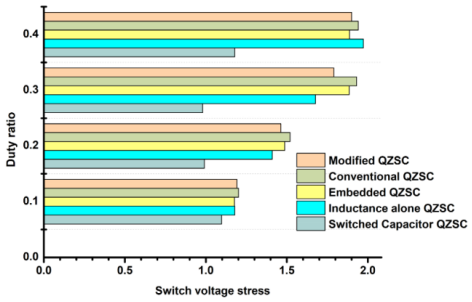


Fig. 14 – Switch voltage stress.

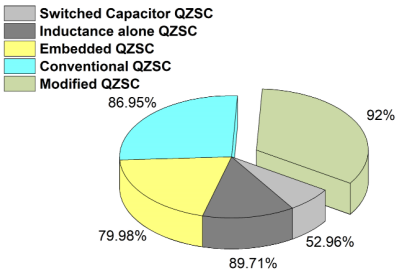


Fig. 15(a) – Efficiency of all the topologies.

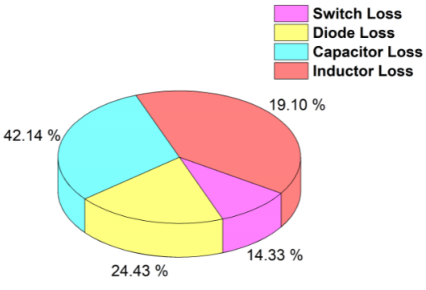


Fig. 15 (b) – Power loss distribution of the proposed topology for $d = 0.15$.

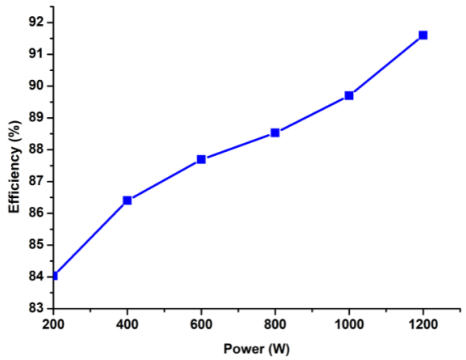


Fig. 15 (c) – Efficiency of the proposed topology versus output power.

4.1 VOLTAGE GAIN

From Fig. 10, it could be observed that the voltage gain characteristics of embedded QZSC and conventional QZSC are identical, and the proposed modified QZSC and inductance alone QZSC have the same voltage gain characteristics. Though the switched capacitor QZSC has a high voltage gain, the gain drops when the duty ratio increases beyond 0.3. Also, the embedded QZSC and conventional QZSC have drooping characteristics. However, the proposed modified QZSC has linear characteristics and has higher voltage gain than embedded QZSC and conventional QZSC.

4.2 OUTPUT VOLTAGE RIPPLE

The output voltage ripples (ΔV_o) of all the converters are presented in Fig. 11. Though the switched capacitor QZSC has high voltage gain as depicted in Fig. 10, the output voltage ripple is very high as shown in Fig. 11. But, the suggested modified QZSC has low output voltage ripple for all the values of duty ratio compared with other topologies.

4.3 CAPACITOR VOLTAGE STRESS

The comparison of capacitor voltage stress for all the values of duty ratio is presented in Fig. 12. From Fig.12, it could be implied that the embedded QZSC has very high capacitor voltage stress, whereas, switched capacitor QZSC has low V_{cs}. But, the suggested modified topology has low capacitor voltage stress compared with embedded QZSC and conventional QZSC. In inductance alone QZSC, as there is no capacitor in the network, the voltage stress across the capacitor is eliminated.

4.4 NETWORK DIODE VOLTAGE STRESS

The network diode voltage stress of all the five topologies is shown in Fig. 13. The recommended modified topology has low network diode voltage stress compared with embedded QZSC and conventional QZSC, but modified QZSC has high V_{ds} than the switched capacitor QZSC and inductance alone QZSC as depicted in Fig. 13.

4.5 SWITCH VOLTAGE STRESS

The switch voltage stress is presented in Fig. 14. From Fig.14, it can be observed that the suggested topology has low switch voltage stress compared with all other topologies except the switched capacitor QZSC.

4.6 EFFICIENCY

The pictorial representation of the efficiency of all five topologies is shown in Fig. 15 (a). The presented efficiency digital data is calculated for the duty ratio of 0.15. The proposed topology's output power (Pout) is 1099.31W, and the power loss (P_{loss}) is 95.04 W; thus, an efficiency of 92% has been obtained. Fig. 15 (b) shows the power loss distribution of the proposed converter for the duty ratio of 0.15, and Fig. 15 (c) depicts the variation of the proposed converter efficiency for different output power values.

Figure 15 shows the suggested modified topology is more efficient than existing topologies. Also, the efficiency increases for different output power values. It has been observed from the results that the modified QZSC has superior performance, such as linear voltage gain characteristics, reduced output voltage ripple, reduced stress, and high efficiency. The comparative analysis of all five topologies for the specified duty ratio of 0.15 is listed in Table 2. The number of diodes, inductors, and capacitors is represented as N_D, N_L, and N_C.

From Table 2, it could be implied that the suggested modified QZSC has reduced output voltage ripple and improved efficiency compared with all other topologies. Though conventional QZSC's and modified QZSC's voltage gain are the same, all other parameters are improved with the modified QZSC. The stress across the network and the switch is reduced with the switched capacitor topology. However, the topologies have high output voltage ripple and require more passive components. This does not exist in the modified topology.

Moreover, the voltage gain characteristics of the recommended converter topology are linear, whereas other topologies have drooping characteristics. Thus, it is proven that the performance of the suggested modified topology is superior compared with other topologies. Finally, the five topologies' advantages and drawbacks are presented in Table 3.

Table 2

Comparison of converter topologies

QZSC Topology	Voltage gain (G)	Output voltage ripple (ΔV_o) (%)	$V_{cs} = \left(\frac{V_c}{V_i}\right)$	$V_{ds} = \left(\frac{V_d}{V_i}\right)$	$V_{ss} = \left(\frac{V_s}{V_i}\right)$	Efficiency (%)	N_D	N_L	N_C
Switched capacitor	1.49	15	0.073	0.52	0.5	52.96	3	3	5
Inductance alone	1.26	1.4	Nil	0.84	1.29	89.71	3	3	1
Embedded	1.29	1.9	1.15	1.15	1.31	79.98	2	3	3
Conventional	1.3	2.1	0.16	1.18	1.34	86.95	2	2	3
Modified	1.3	1.4	0.14	0.99	1.32	92	3	2	2

Table 3

Comparison of converter topologies

QZSC Topology	Advantages	Drawbacks
Switched capacitor	High voltage gain and reduced stress	Drooping voltage gain characteristics and low efficiency
Inductance alone	Low voltage ripple	Low efficiency
Embedded	High voltage gain	High voltage ripple and low efficiency
Conventional	Reduced switch stress	Drooping voltage gain characteristics
Modified	Linearly high voltage gain, reduced stress and high efficiency	Requirement of diode component is high

5. EXPERIMENTAL RESULTS OF THE PROPOSED TOPOLOGY

A 60 W laboratory setup has been developed to verify the performance of the suggested converter. The triggering pulse is generated using ARDUINO UNO, where the switching frequency is 25 kHz and the duty cycle is 0.15. The parameter

specifications are V_{in} = 40 V, V_0 = 52 V, L = 147 μH, and C_1 = C_0 = 416 μF. The power switch is MOSFET (IRFP 250) along with the driver circuit, and the diode is FR107. The prototype setup is depicted in Fig. 16. Two dc voltage sources are cascaded to provide a supply voltage of 40 V. The output is measured using a power quality analyzer WT500.

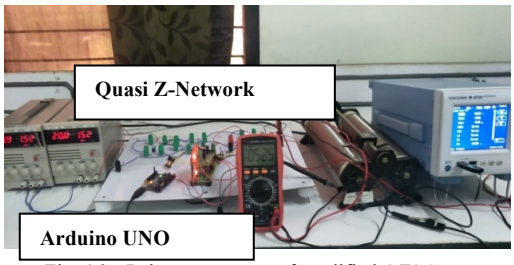


Fig. 16 – Laboratory setup of modified QZSC.

From Fig.16, it could be identified that the source voltage of 40 V is stepped up to 52.5 V for the duty cycle of 0.15. The measured output waveform and stress waveform are presented in Figs. 17 to 20.

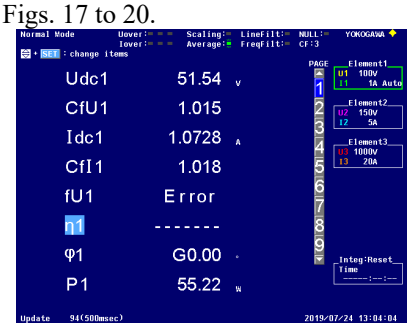


Fig. 17 – Output voltage ripple (CfU1) and output current ripple (CfI1).

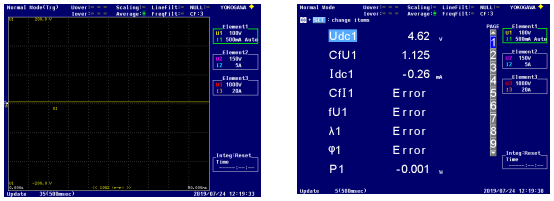


Fig. 18 – Average value of capacitor voltage.

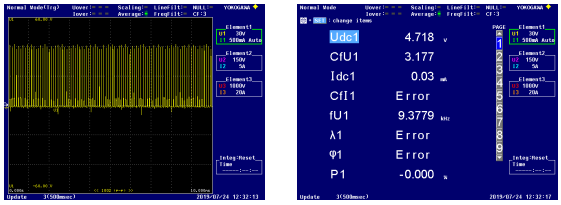


Fig. 19 – Average value of diode voltage.

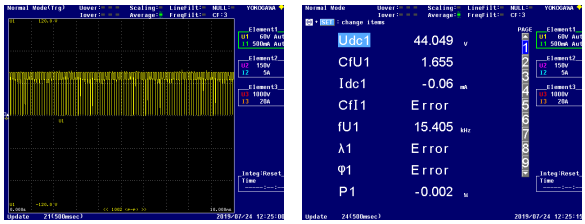


Fig. 20 – Average value of switch voltage.

6. DISCUSSION AND INTERPRETATIONS

The results in section 4 clearly show that the switched capacitor topology has high performance, such as high voltage gain and reduced stress. Still, it has high output voltage ripple and low efficiency compared to other topologies. Comparatively, the switched capacitor QZSC requires more passive elements. Moreover, the voltage gains of all the reviewed topologies, except modified QZSC and inductance alone QZSC, drop when the duty ratio increases beyond 0.3. Though the conventional QZSC and embedded QZSC have the same voltage gain and output voltage ripple values, the embedded QZSC possesses high V_{cs}, and conventional QZSC possesses high V_{ds} and V_{ss}. This has been overcome in the proposed modified topology, and the output voltage ripple of modified QZSC is low compared with conventional QZSC. Also, in section 4, it has been observed that the characteristics of inductance alone QZSC and modified QZSC are similar. However, the efficiency of the suggested topology is superior against the inductance alone QZSC. Overall, the recommended modified quasi-Z-source converter's performance remains better than all other topologies.

7. CONCLUSION

The different topologies of a quasi-Z-source converter, such as a conventional, embedded, switched capacitor, inductance alone, and the proposed modified topology, have been reviewed and analyzed. The circuit diagram and the modes of operation of all the topologies are presented. The performance of all five topologies is evaluated and compared. The parameters are voltage gain (G), output voltage ripple (ΔV_o), network capacitor voltage stress (V_{cs}), network diode voltage stress (V_{ds}), switch voltage stress (V_{ss}), efficiency (Ƞ), and the number of passive components has been computed for different values of duty ratio. It has been inferred from the analysis that the suggested topology has a low ripple in output voltage compared with all other topologies. The stress across the network of modified QZSC and switch voltage stress is also less compared with embedded QZSC and conventional QZSC. The efficiency of the proposed QZSC is superior to other existing quasi-Z-source converters.

Moreover, the voltage gain of the proposed topology does not drop when the duty ratio increases. Also, the proposed topology requires a smaller number of passive elements and, thus, minimizes the power loss. The behavior of both modified QZSC and inductance alone QZSC are identical, but the efficiency is improved with modified topology compared with inductance alone QZSC. Hence, the proposed quasi-Z-source converter is chosen as it has better performance. A laboratory setup has been developed to verify the theoretical values. The prototype model has been tested with a dc voltage source of 40 V that is stepped up to 52.2 V for the duty ratio of 0.15. The suggested topology has an output voltage ripple of 1%, network capacitor voltage stress (V_{cs}) of 0.11, network diode voltage stress (V_{ds}) of 0.11, switch voltage stress (V_{ss}) of 1.1, and efficiency of 92 %. Thus, the simulation results are validated.

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