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A NOVEL FAULT-TOLERANT ASYMMETRICAL 21-LEVEL INVERTER TOPOLOGY WITH REDUCED COMPONENTS

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The foremost objective of this work is to propose a fault-tolerant (FT) asymmetrical 21-level inverter with minimal power semiconductor switches and voltage sources. The topology of the proposed inverter is to produce high voltage levels with low harmonic content and minimize electromagnetic interference (EMI) in the system. Meanwhile, the novelty has been proved by a detailed comparison between the suggested multilevel inverter (MLI) and recently introduced topologies using several components such as switches, capacitors, sources, gate driving circuits, total standing voltage (TSV), component count per level and cost function. Additionally, the flexible circuit connection between sources, switches, and loads provides the alternative configuration for 21-level MLI to operate as a 9-level and 7-level MLI topology, ensuring FT capability during the failure of specific sources and switches. The nearest voltage level (NVL) algorithm technique produces gate driver signals for the switches, which generate high-quality waveform compared to other pulse width modulation (PWM) techniques. A simulation model is designed to support the simulation results using MATLAB/Simulink software and hardware implementation. The results are analyzed under different combinations of linear and nonlinear loads. In both simulation and experiment, the evaluated parameter values show good performance concerning other structures, and total harmonic distortion (THD) is less than 5 % as per IEE519 standards.

1. INTRODUCTION

Due to the depletion of fossil fuels, climate change, and green power demand, photovoltaic (PV) solar panels are replacing conventional power plants to produce electrical energy. As per recent data, the total solar generation exceeds 220 GW installed rating worldwide [1,2]. Apart from that, the greenhouse gas emission of conventional vehicles is eliminated by electrical transportation operated with the help of a battery and alternating current (ac) fed electrical drives [3-4]. In both cases, the nature of the energy source is direct current (dc), but most of the domestic load, industrial equipment, and drives are ac in nature. So, we need a suitable power electronic conversion device to change the waveform from dc to ac for grid synchronization or direct source applications. Nowadays, the two-level or square inverter is mainly used to convert from dc to square-type sinusoidal waveform at the high switching frequency and is used for applications such as standalone systems and low-power energy consumption devices. In addition, its poor performance is validated by conversion parameters such as high total harmonic distortion, high switching stress, high dv/dt, electromagnetic interference, and other reliability issues. So, to overcome the limitations, a new highly efficient and intelligent power conversion device, a multi-level inverter, has been introduced [5,6]. It comprises medium voltage semiconductor switches and sources such as batteries, solar panels, and supercapacitors. It produces the staircase-type sinusoidal waveform containing higher voltage levels at the low switching frequency, leading to lower switching losses, higher efficiency, low voltage stress, and low THD value.

Such merits make the MLI gain attention for high power and voltage systems. However, the challenges are that several switches and sources requirement is high, it makes the topology and its control circuits more complex. Industrial power electronics companies like ABB, General Electric, Siemens, etc., have used MLI in their power conversion equipment. Based on source value, it is classified into symmetrical, asymmetrical, and hybrid multilevel inverters. An equal magnitude of voltage sources is used in symmetrical topology, while unsymmetrical have unequal voltage sources.

Based on the configuration, the classical classification of MLI is diode clamped (DC-MLI), flying capacitors (FC-MLI), and cascaded H-bridge (CHB-MLI). The circuit connection and its various inevitable issues, such as voltage balancing, modularity, low efficiency, switch control, and a higher number of components of classical topologies, is discussed [7]. In this perspective, our researchers recently introduced a different configuration to increase the number of levels while decreasing component counts to reduce the problems faced with classical topologies [8–16]. An asymmetrical multilevel inverter is introduced [10]. It contains 14 switches, 2 sources, and 2 capacitors to produce 21 levels MLI, although it needs a complex controller for voltage balancing issues due to the employment of capacitors. In literature [11], another 21-level asymmetrical inverter is proposed, which contains 10 switches, 6 sources, and 3 capacitors. The configuration used in [12] utilizes 12 switches and 3 sources.

Further, to generate switching pulses for power semiconductor devices in MLI, different pulse width modulation (PWM) techniques are used, such as space vector modulation (SVM), selective harmonic elimination (SHE-PWM), sinusoidal pulse width modulation (SPWM) is analyzed and compared. It reduces harmonic content and gives high-quality output waveform. A fault-tolerant has been introduced that operates in lower levels, even failure of specific sources and switches [17,18].

Based on these studies, there is a gap in optimizing the device count; this work proposes a novel fault-tolerant asymmetrical inverter to produce 2l voltage levels with the help of 10 unidirectional power switches and three sources. The above survey proves the novelty of the proposed topology in terms of reduced components to generate the same voltage levels as related to recently introduced topologies. It is appropriate for applications such as ac fed Electrical drives, flexible alternating current transmission systems (FACTS), Renewable solar energy integration,

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uninterruptible power supply (UPS), *etc*.

The remaining part of the paper is systematized as follows; Section 2 explains the operating modes of the proposed 21-level inverter using insulated gate bipolar transistor (IGBT) switches and trinary voltage sources. The fault-tolerant ability of the inverter under specific source and switch failures is investigated in section 3. Section 4 elaborates and analyzes the comprehensive comparison of proposed MLI with recently introduced topologies to prove its superiority in terms of performance parameters. Finally, Section 5 comprises the simulation results of the proposed concept by MATLAB/Simulink environment and hardware prototype set up in the laboratory and then compares its performance parameters. Section 6 concludes the proposed concept.

2. PROPOSED INVERTER TOPOLOGY

Figure 1 depicts the suggested 21-level asymmetric multilevel inverter structure. Ten unidirectional electronic power switches and three asymmetric dc voltage sources constitute the proposed inverter. The voltage magnitude, V_{dc}, is selected based on the trinary ratio of 6:3:1 to create a 21-level output voltage. The current flow path during positive and negative modes of operation is demonstrated in Fig. 2. For $10V_{dc}$, switches S_1, S_4, S_5, S_7, and S_{10} turn on, forming the path (V_1-S_4-V_2-S_5-S_{10}-V_3-S_7-L-S_1-V_1) where sources V_1, V_2, V_3 act in circuit and yield total voltage of ($V_1 + V_2 + V_3$).In $9V_{dc}$, the switches S_1, S_4, S_5, S_8, S_{10} form the path (V_1-S_4-V_2-S_5-S_{10}-S_8-L-S_1-V_1), the voltages V_1, V_2 are connected in the circuit get a total voltage of (V_1+V_2).

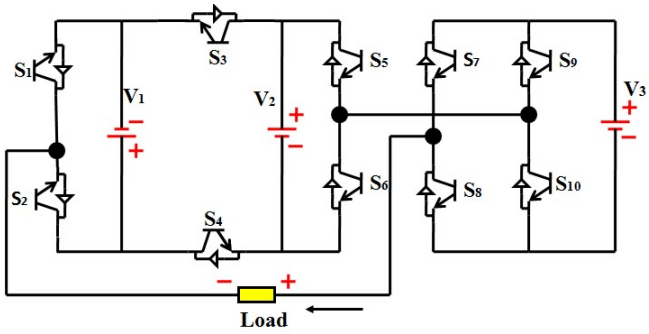


Fig. 1 - Proposed 21-level inverter.

In $8V_{dc}$, the switches S_1, S_4, S_5, S_8, and S_9 turn on, and the positive polarity of sources V_1, V_2 and the negative polarity of source V_3 are connected to obtain a voltage of (V_1+V_2-V_3). In $-V_{dc}$, the switches S_2, S_4, S_6, S_8, S_9 turn on, negative polarity of V_3 is connected to get a voltage of –(V_3). In $-2V_{dc}$, switches S_1, S_3, S_6, S_7, S_{10} turn on, source V_2 and V_3 act in circuit and produce –(V_2-V_3).

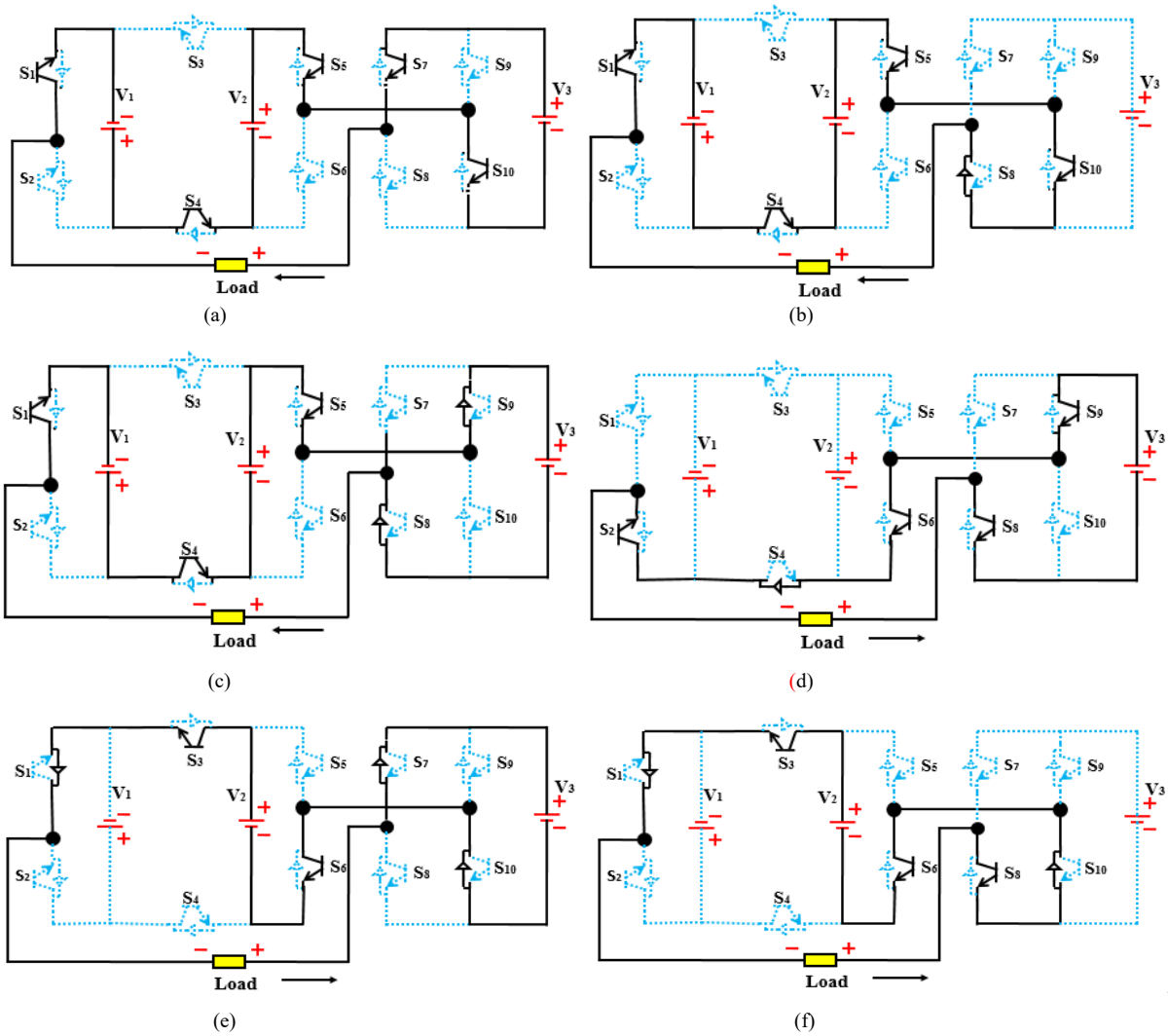


Fig. 2 – Current flow path for different modes; (a) $V_1 + V_2 + V_3$; (b) V_1+V_2 ; (c) V_1+V_2-V_3 ; (d) –(V_3) ; (e) –(V_2-V_3) ; (f) –(V_2).

Similarly, the different switching states generate different voltage levels for positive and negative polarity waveforms and are given in Table 1.

Table 1

Switching States

Output Voltage	On-State Switches	
	Positive Cycles	Negative Cycles
0	S_2, S_4, S_6, S_8, S_{10}	S_2, S_4, S_6, S_8, S_{10}
V_{dc}	S_2, S_4, S_6, S_7, S_{10}	S_2, S_4, S_6, S_8, S_9
$2V_{dc}$	S_2, S_4, S_5, S_8, S_9	S_1, S_3, S_6, S_7, S_{10}
$3V_{dc}$	S_2, S_4, S_5, S_8, S_{10}	S_1, S_3, S_6, S_8, S_{10}
$4V_{dc}$	S_2, S_4, S_5, S_7, S_{10}	S_1, S_3, S_6, S_8, S_9
$5V_{dc}$	S_1, S_4, S_6, S_8, S_9	S_2, S_3, S_5, S_7, S_{10}
$6V_{dc}$	S_1, S_4, S_6, S_8, S_{10}	S_2, S_3, S_5, S_8, S_{10}
$7V_{dc}$	S_1, S_4, S_6, S_7, S_{10}	S_2, S_3, S_5, S_8, S_9
$8V_{dc}$	S_1, S_4, S_5, S_8, S_9	S_2, S_3, S_6, S_7, S_{10}
$9V_{dc}$	S_1, S_4, S_5, S_8, S_{10}	S_2, S_3, S_6, S_8, S_{10}
$10V_{dc}$	S_1, S_4, S_5, S_7, S_{10}	S_2, S_3, S_6, S_8, S_9

The switch pulses are generated by the nearest voltage level algorithm technique (NVL). It senses the reference signal and produces the stepped waveform per switching states. This technique is suitable for higher levels in terms of harmonic distortion.

3. FAULT-TOLERANT TOPOLOGY

The fault-tolerant capability of the proposed MLI is analyzed in this section. The general faults F in MLI are source failure, semiconductor switch open or short circuit, and gate driver circuits malfunction due to excessive thermal stress. In this paper, the failure of specific switches and sources is focused. In case of the open circuit of switches (S_7 or/and S_9) or/and failure of sources V_3, the inverter operates as 7-level MLI without any change in circuit connection. But fault tolerant strategy depends on new voltage reference and switching states to maintain power quality standards for loads. The voltage magnitude V_1 and V_2 operates in the ratio of 2:1. In the same manner, the short circuit of switches (S_1 or/and S_3) or/and failure of sources V_1, the inverter again able to exhibit 9 level MLI. The voltage magnitude V_2 and V_3 operates in the ratio of 3:1, respectively. Table 2 and Table 3 provide the switching states for MLI at 7 levels and 9 levels, respectively.

Table 2

Switching states of 7-level MLI*

V_o	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}
$9V_{dc}$	1	0	0	1	1	0	F	1	F	1
$6V_{dc}$	1	0	0	1	0	1	F	1	F	1
$3V_{dc}$	0	1	0	1	1	0	F	1	F	1
$0V_{dc}$	1	0	1	0	1	0	F	1	F	1
$-3V_{dc}$	1	0	1	0	0	1	F	1	F	1
$-6V_{dc}$	0	1	1	0	1	0	F	1	F	1
$-9V_{dc}$	0	1	1	0	0	1	F	1	F	1

* V_1 or/and S_7, S_9 open circuit failure

Table 3

Switching states of 9 level MLI*

V_o	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}
$4V_{dc}$	F	F	0	1	1	0	1	0	0	1
$3V_{dc}$	F	F	0	1	1	0	0	0	0	1
$2V_{dc}$	F	F	0	1	1	0	0	0	0	0
$1V_{dc}$	F	F	0	1	0	0	1	0	0	1
$0V_{dc}$	F	F	1	0	1	0	0	0	0	1
$-1V_{dc}$	F	F	0	0	0	1	0	1	1	0
$-2V_{dc}$	F	F	1	0	0	1	0	0	0	0
$-3V_{dc}$	F	F	1	0	0	1	0	1	0	0
$-4V_{dc}$	F	F	1	0	0	1	0	1	1	0

* V_1 or/and S_1, S_2 short circuit failure

4. COMPARISON STUDY

Table 4 compares the performance of the proposed 21-level MLI asymmetrical architecture with other recently introduced MLI to demonstrate its novelty. The parameters considered are Total harmonic distortion (THD), Number of levels (N_L), Number of switches (N_S), Gate driver board circuits (N_{GD}), DC sources (N_{DC}), Cost function per level (CF/L), Number of Capacitors (N_C), Number of diodes (N_D), Components count per level (CCpL) are used for comparison. The component count per level (CCpL) is estimated by applying [13]

$$CCpL = \frac{N_S + N_D + N_C + N_{GD} + N_{DC}}{L}, \quad (1)$$

By reducing the number of components needed to configure topology concerning the chosen level, the value of CCpL is decreased. This, in turn, minimizes circuit complexity, switching losses, and cost and enhances overall efficiency.

The cost function is found by using [14]

$$Cost \text{ Function} = (N_S + N_{GD} + \alpha TSV) \times N_{DC}, \quad (2)$$

where α is the current coefficient factor. The value α is selected as either α > 1 or α < 1 to explore the wide variation of the cost function. The standing voltage (SV) is the maximum blocking voltage of the switch during the off state. The sum of the standing voltage for power semiconductor devices in the proposed topology evaluates the total standing voltage (TSV). The generalized equation for voltage of unidirectional, bidirectional switches and TSV is given in [14]

$$TSV = \mathrm{SV}_1 + \mathrm{SV}_2 + \mathrm{SV}_3 + ... + \mathrm{SV}_{N_S}, \quad (3)$$

$$TSV = \sum_{i=1}^{N_S} \mathrm{SV}_i, \quad (4)$$

where N_s is the number of switches. The total standing voltage per level is the ratio of TSV to the number of levels. It is used for comparing voltage stress across switches.

Table 4

Comparison of performance parameters

Topology	N_S	N_{GB}	N_{DC}	TSV	CCpL	Cost function	
						α = 0.5	α = 1.5
14	14	12	2	2	4.89	1.52	3.10
13	12	12	5	4.42	1.26	6.8	7.9
12	12	12	3	4.27	1.17	3.4	3.96
11	12	10	3	4.43	1.19	3.5	4.08
10	12	12	3	4.57	1.28	3.8	4.34
9	10	10	6	4.02	1.38	10	11.14
8	14	13	2	4.34	1.47	4.22	4.51
Proposed	10	10	3	4.23	1.09	3.16	3.76

As per Table 4, the proposed topology has fewer total components, leading to less CCpL and cost function.

5. RESULTS AND DISCUSSION

The theoretical aspects of the proposed 21-level inverter topology are proved by simulating in MATLAB/Simulink software environment. Output waveforms and their THD analyze the performance under dynamic load conditions. The asymmetrical inverter topology comprises three unequal dc voltage sources with ten IGBT power semiconductor switches. The voltage magnitudes are chosen as V1 = 198 V, V2 = 99 V, and V_3 = 33 V. The gate pulses are generated per switching states with the help of the nearest voltage level (NVL) algorithm technique by considering a 50 Hz sinusoidal waveform as a reference. The switching pulses, 21-level voltage waveform,

current waveform, and fast Fourier transform (FFT) analysis for pure resistive load R are revealed in Fig. 3.

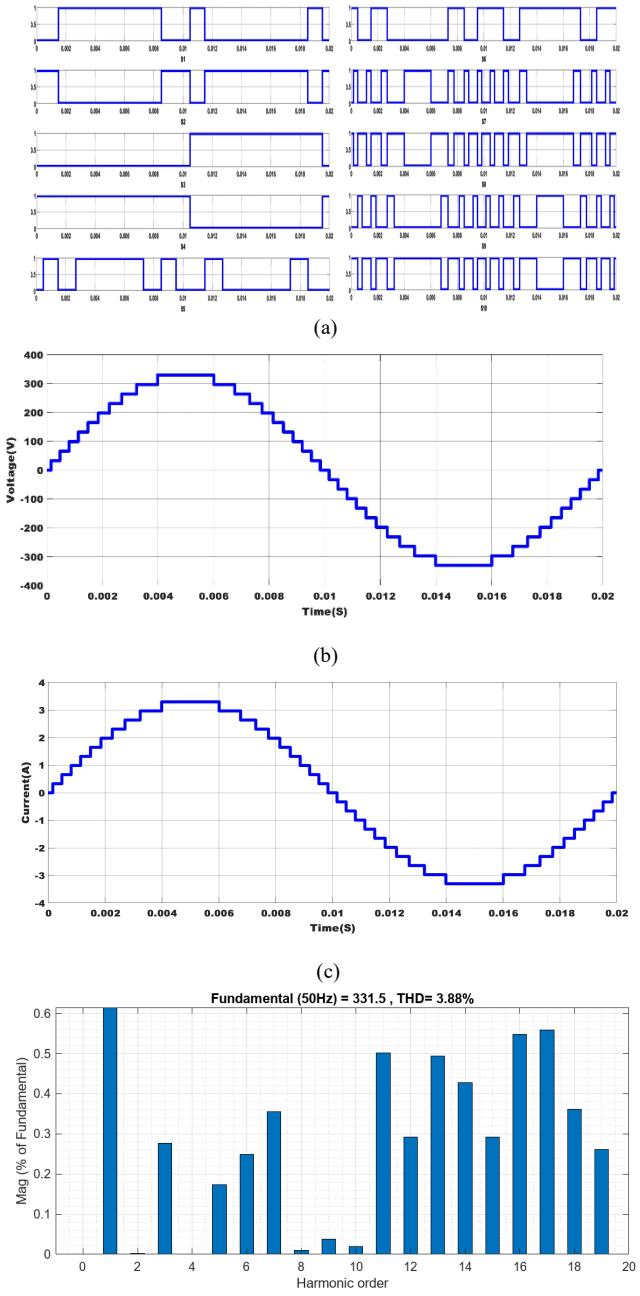


Fig. 3 - Simulation results of 21-level MLI; (a) Switching pulses; (b) Waveform of the output voltage for R = 100 Ω; (c) Waveform of the output current for R = 100 Ω; (d) FFT analysis of 21-level output voltage waveform for R = 100 Ω.

As per the electrical parameters for sources and loads, we get the maximum voltage, maximum current, and THD is 330 V, 3.3 A, and 3.88 % for a resistive load of 100 Ω. The low value of THD satisfies IEEE 519 standards (THD < 5 %) and eliminates the filter requirements, which minimizes the size and cost of the system. Further, the faults are introduced in the configuration, and its fault-tolerant capability is analyzed. The 21-level topology produces 9-level under the short circuit of switches (S_1 or/and S_3) or/and failure of sources V_1. Similarly, it produces 7-level under the open circuit of switches (S_7 or/and S_9) or/and failure of sources V_3. Figure 4 and Fig. 5 illustrate the pulses, waveform, and FFT analysis for 9 levels and 7 levels, respectively.

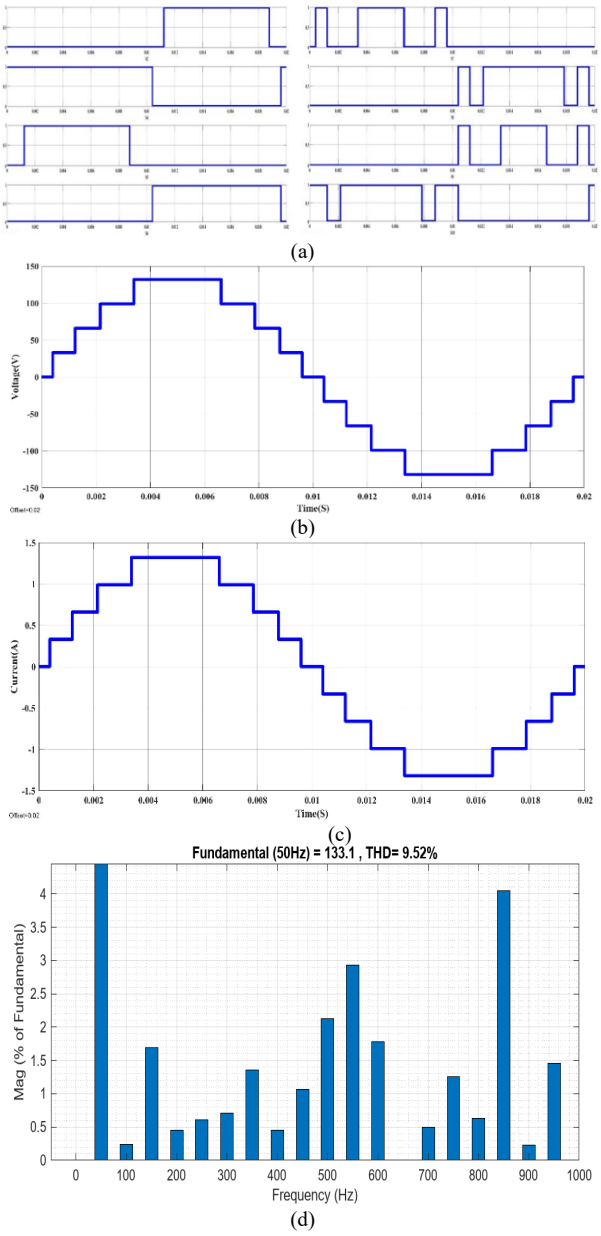
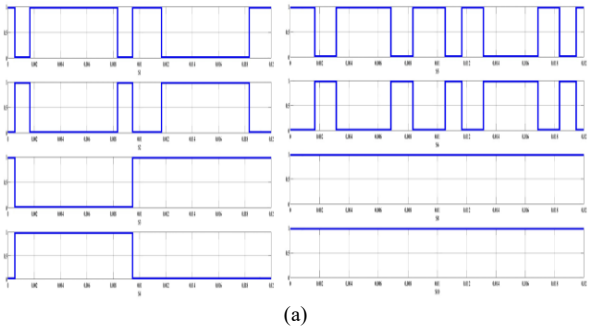


Fig. 4 – Simulation results of 9-level MLI; (a) Switching pulses; (b) Waveform of the output voltage for R = 100 Ω; (c) Waveform of the output current for R = 100 Ω; (d) FFT analysis of 9 level output voltage waveforms for R = 100 Ω.

The THD value of the load voltage and load current waveform for 21-level, 9-level, and 7-level inverters are given in Table 5, Table 6, and Table 7, respectively. It shows the variation of harmonic value for pure resistive, resistive and inductance, and pure inductance loads. The harmonics change is more minor for different combinations of loads.



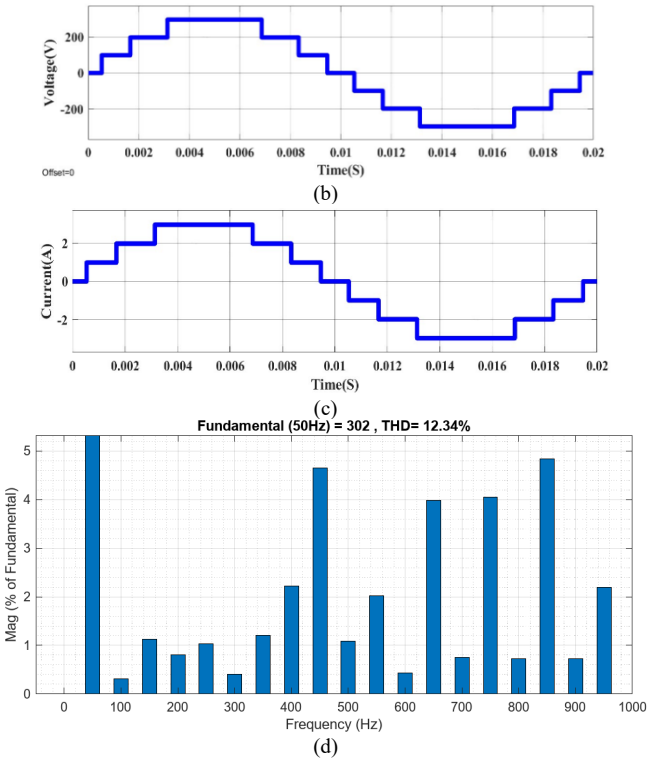


Fig. 5 – Simulation results of 7-level MLI; (a) Switching pulses; (b) Waveform of the output voltage for R = 100 Ω; (c) Waveform of the output current for R = 100 Ω; (d) FFT analysis of 7-level output voltage waveform for R = 100 Ω.

Table 5

Load variation analysis of 21-level MLI

S. No	Load	Load current THD (%)	Load voltage THD (%)	Power factor
1	2000 mH	0.15 %	3.82 %	0
2	100 Ω & 1558 mH	17.72 %	3.80 %	0.2
3	100 Ω & 551 mH	20.82 %	3.82 %	0.5
4	100 Ω & 238 mH	14.20 %	3.79 %	0.8
5	100 Ω	3.82 %	3.82 %	1

Table 6

Load variation analysis of 9-level MLI

S. No	Load	Load current THD (%)	Load voltage THD (%)	Power factor
1	2000 mH	0.30 %	9.26 %	0
2	100 Ω & 1558 mH	14.34 %	9.18 %	0.2
3	100 Ω & 551 mH	17.23 %	9.48 %	0.5
4	100 Ω & 238 mH	12.43 %	9.42 %	0.8
5	100 Ω	9.48 %	9.48 %	1

Table 7

Load variation analysis of 7-level MLI

S. No	Load	Load current THD (%)	Load voltage THD (%)	Power factor
1	2000 mH	0.49 %	12.04 %	0
2	100 Ω & 1558 mH	17.85 %	11.85 %	0.2
3	100 Ω & 551 mH	21.11 %	12.22 %	0.5
4	100 Ω & 238 mH	14.24 %	12.14 %	0.8
5	100 Ω	12.22 %	12.22 %	1

Further, to validate the simulated results, a hardware prototype is developed in the laboratory, which comprises IGBT 25N120, 600 V, 25 A IGBTs, gate driver circuits (TLP250, IC7815, and other necessary electrical devices), and three asymmetrical dc power supplies are designed using a transformer and dc-dc converter. The experimental setup is displayed in Fig.6.

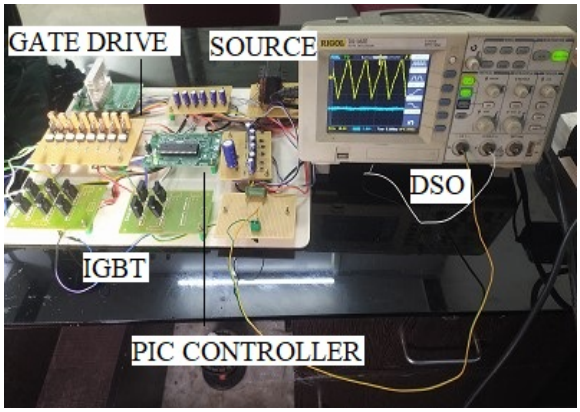


Fig. 6 – Experimental setup of 21-level MLI.

The gate driver signals for IGBT are generated with the help of controller board PIC 16F887, according to Table 1. The voltage waveform of the 21-level inverter captured using a digital oscilloscope is shown in Fig.7.

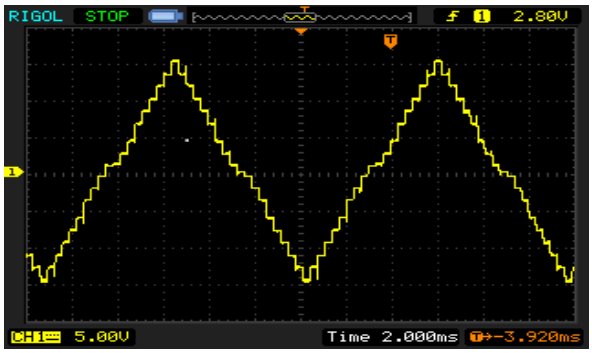


Fig. 7 – Experimental results of 21-level MLI.

Then its results are compared and confirmed that the experimental outputs are approximately identical to the simulated results. A slight deviation is produced due to noise disturbance in practical application.

6. CONCLUSIONS

A novel fault-tolerant 21-level asymmetrical inverter topology has been proposed in this paper. The proposed topology comprises ten unidirectional switches and three asymmetrical DC voltage sources. The important values are THD = 3.88 %, TSV_{pu} = 4.23, CCpL = 1.09, and cost function as 3.16 and 3.76 for α = 0.5 and α = 1.5, respectively. Further, the detailed comparison shows that the performance of the proposed MLI is superior to recently introduced topologies, and THD is less than 5 % as per IEEE 519 under linear and nonlinear loads. The reliability of the MLI system has improved by FT capability 21-level topology, which modifies as 9-level and 7-level inverter topologies to maintain continuity of power supply under specific fault conditions. It suits applications like PV solar energy integration, electric vehicles, and FACTS controllers.

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