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AN ULTRA-CAPACITOR INTEGRATED DYNAMIC VOLTAGE RESTORER FOR POWER QUALITY ENHANCEMENT IN A THREE-PHASE DISTRIBUTION SYSTEM USING AN ADAPTIVE NEURO-FUZZY INTERFERENCE SYSTEM CONTROLLER

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Keywords: Power quality (PQ); Dynamic voltage restorer (DVR); Voltage sag; Voltage swell; Adaptive neuro-fuzzy interference system (ANFIS) controller; Ultracapacitor; Synchronous reference frame theory.

Power quality voltage-related issues sag and swell are recognized as recurrent, severe threats in the distribution systems that lead to an enormous loss in productivity and profitability for both utilities and customers. Dynamic voltage restorer (DVR) is a well-known commercial solution for the issues of sag and swell. There has been an enhanced interest in incorporating Renewable energy resources into the dc input source of custom power devices. The chosen energy storage device should be capable of affording peak power with less duration. Ultracapacitors (UCAPs) are the better choice for energy storage with less cost and are also suited for mitigating sag and swell issues, which need enormous power with minimum duration. The novelty of this paper is its contribution to the design of an integrated renewable UCAP energy storage device as a dc source for DVR (UCAP-DVR). An improved synchronous reference frame (SRF) algorithm with an adaptive neuro-fuzzy interference system (ANFIS) controller is employed to enhance the compensation capability of the UCAP-DVR system against unbalanced sag and swell problems. It also provides active power support to the grid. This integration proposes a suitable bidirectional converter to afford a stiff DC input voltage for DVR. Many complications in designing and controlling the voltage source inverter (VSI) and the proposed converter are discussed. The proper integration of UCAP-DVR with the distribution grid using the SRF-ANFIS Controller was done in MATLAB simulation. The behavior of the proposed DVR for the problems of both balanced and unbalanced voltage sag and swell was discussed. A comparison has been made with the SRF-PI controller to outline the importance of the proposed controller for UCAP-DVR. Hardware experimental setup of this integrated UCAP-DVR system is developed, and the ability to provide voltage sag and swell compensation in all three phases to the distribution grid is dynamically tested successfully.

1. INTRODUCTION

Power quality (PQ) in the distribution system [1] and their solutions have received much attention in recent years. They have become a concern in modern industrialized and marketable applications. Complicated loads from various industries and utility-side distribution power networks are all disturbed by different PQ issues [2,3], such as voltage sag, swell, harmonics, *etc*. Among the PQ problems, many researchers have proven that sag and swell issues [3] are the largest harsh, frequently occurring faults in the distribution system.

The dynamic voltage restorer (DVR) is a custom power device [4,5], and it has provided a standard economical solution for all kinds of sag, swell problems, and Harmonics [6]. The alleviation ability of DVR mostly depends on its maximum magnitude of voltage injection capacity [7,8] and its contribution to providing active power. Generally, battery energy storage is used as an input for DVR [9] to provide active power, but batteries are still bulky and costly. They must be disposed of once their chemicals are used up, which limits the compensation capability of DVR. In the present years, there is an enormous growth in the consumption of power which has motivated researchers to spotlight more on renewable energy sources (RES). Many researchers are interested [10,11] in suggesting a rechargeable energy storage device as an alternative to a battery at the input source of STATCOM, DVR.

The ultra-capacitor (UCAP) based energy storage devices fulfill the above requirement [12,13]. UCAP's have numerous prospective advantages that formulate them in a lot of applications because they don't have moving parts; it is safe from chemical reaction. Many researchers suggested different types of intelligent controllers [14], such as fuzzy logic [15–18] to enhance the performance of DVR.

This paper proposes a novel DVR topology by introducing a renewable energy storage device ultra-capacitor as a dc input to DVR; this maintains its dc link voltage and affords active power support to the grid. The results prove that this integrated UCAP-DVR design is an excellent alternative for maintaining its dc input voltage and providing active power support to the grid. In the controller part, an improved Synchronous Reference Frame (SRF) Theory control algorithm [19–21] is proposed along with ANFIS controller [22,23], which was proven to compensate for both balanced and unbalanced PQ problems. A suitable buck–boost converter is designed and implemented in simulation. Therefore, the ultracapacitor charges up during a swell event, and during a sag event, it supplies voltage. Thus, the DVR dc link voltage is regulated as constant during compensation. This improves its compensation capability. The proposed UCAP-DVR is tested for various depths of both balanced and unbalanced sag and swell issues. The comparison with SRF-PI and FUZZY controllers defines the importance of the proposed SRF-ANFIS controller.

This paper is organized into five sections. The operation of UCAP based DVR is expounded in section 2. The design and modeling of UCAP module is presented in section 3. The ANFIS controller and the SRF control algorithm implementation is enumerated in section 4. The modeling and simulation results of the proposed model are deliberated in section 5. The hardware impletion of the proposed model is presented in section 6. Finally, the

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conclusion of the paper finds a place in section 7.

2. UCAP-DVR INTEGRATED GRID SYSTEM

The schematic model of the UCAP-DVR interconnected with the distribution grid using SRF-ANFIS controller is shown in Fig. 1. Voltage-related PQ issue sag voltage is created by simulating three phases to ground fault, and the addition of capacitive load at the load side of the distribution grid simulates the swell voltage. The DVR's voltage source inverter (VSI) injects an essential voltage to the distribution grid in series to maintain the magnitude of load side voltage undisturbed.

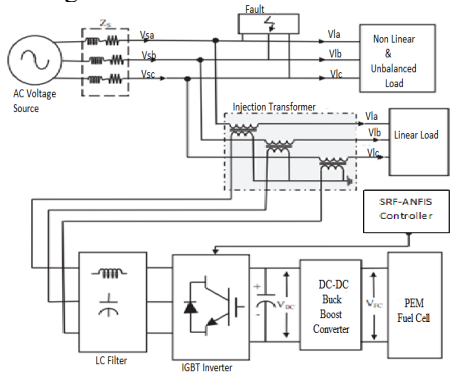


Fig. 1 – UCAP integrated DVR system.

In this proposed DVR configuration, an ultracapacitor is used as dc input; it affords additional power during sag. It consists of UCAP as an energy storage device, DVR, and the bidirectional DC-DC converter. This UCAP-DVR topology can provide and take up real power. Thus grid power is maintained constant. The converter works in boost mode, while the grid gets energy from UCAP, and buck mode, while the grid supplies extra power to UCAP. Fast voltage compensation happens because of the fast charging and discharging capability of UCAP. SRF also enhances the functioning of this UCAP-DVR-ANFIS controller to improve the accuracy of compensation for PQ issues.

3. DESIGN OF ULTRACAPACITOR

The energy storage device UCAP fulfills the gap between the capacitor and the battery. The UCAP Simulink model is shown in Fig. 2. The proposed UCAP module consists of three UCAP cells, each having an output voltage of 48 V and a capacitance of 165 F. These three cells are connected in series to produce an output voltage of 144 V.

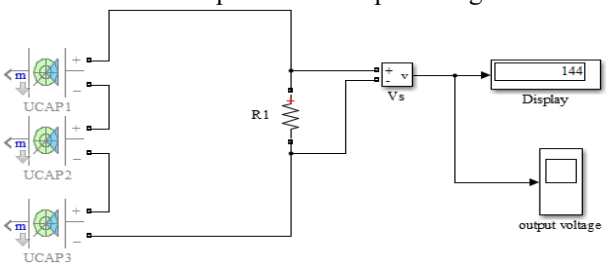


Fig. 2 – UCAP Simulink model.

The converter integrates UCAP with a dc input of DVR to regulate and provides constant dc input for DVR. In this model, the DVR input voltage is chosen as 260V. During the charging mode of UCAP, the converter is working in buck mode; the energy is drawn from the grid used to charge the UCAPs. Thus, the DVR voltage is regulated to 260 V. This UCAP can discharge 50 % of its initial voltage, so the possible voltage discharge of UCAP is from 144 V to 72 V. The converter operates in boost mode when the UCAP output voltage varies from 72 V to 144 V. The buck mode is activated when the UCAP voltage is reduced below 72V. Now, the required energy is drawn from the grid to keep the UCAP output voltage to 260 V, as shown in Fig 3.

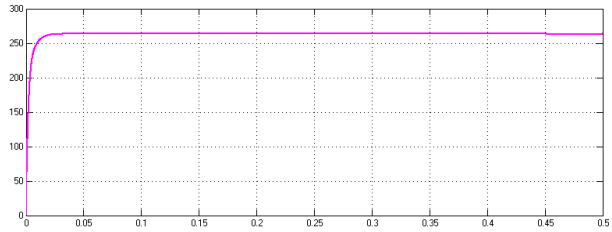


Fig. 3 – DVR dc link voltage.

The design specification of each UCAP cell and dc-dc converter is given in Table 1.

Table 1

Design parameters

Components	Parameters	Values
Ultra-capacitor	Rated capacitance	165 F
	RESR (dc)	7 mΩ
	Rated voltage	48 V
	Leakage current	5.2 mA
	Operating temperature	25 °C
Dc-dc converter	Inductance	181 µH
	Capacitance	44 µF
	Resistance	213.5 Ω
	UCAP Voltage	144 V
Filter	Inductance (L)	1.2 mH
	Capacitance (C)	120 µF

4. ANFIS CONTROLLER IMPLEMENTATION

The SRF control algorithm is used for identifying all symmetrical and unsymmetrical sag and swell issues. This algorithm takes the input DC voltage of DVR and the magnitude of load voltage to estimate direct axis and quadrature axis voltages. The working of the SRF algorithm with the ANFIS controller is shown in Fig. 4.

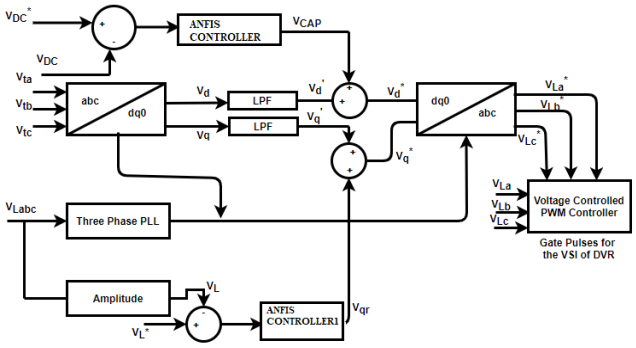


Fig. 4 – SRF control algorithm.

In this theory, the measured three-phase load side voltages are converted from an a-b-c frame to a d-q axis frame using Park's transformation

$$\begin{bmatrix} V_{Tq} \\ V_{Td} \\ V_{T0} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \sin\theta & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \begin{bmatrix} V_{Ta} \\ V_{Tb} \\ V_{Tc} \end{bmatrix}. \quad (1)$$

The phase-locked loop (PLL) locks the phase angle of both load and source voltages. In this algorithm, two ANFIS controllers are used. One is used to control the dc input voltage of DVR. Its output is to produce a loss component of

voltage and is combined with V_d' to generate V_d^*

$$V_d^* = V_d' + V_{cap}, \quad (2)$$

Another ANFIS controller regulates the magnitude of load side voltage; its output voltage is the reactive component of voltage (V_{qr}) combined with V_q to produce reference q axis component load voltage V_q

$$V_q^* = V_q' + V_{qr}. \quad (3)$$

The magnitude of the load voltage is computed as

$$V_L = \sqrt{\left(\frac{2}{3}\right)(V_{La}^2 + V_{Lb}^2 + V_{Lc}^2)}. \quad (4)$$

The resultant d-q axis voltages are transformed to three-phase voltages using reverse Park's transformation in eq. (5). This voltage is a reference voltage for the PWM controller of VSI to produce switching pulses for DVR

$$\begin{bmatrix} V_{La}^* \\ V_{Lb}^* \\ V_{Lc}^* \end{bmatrix} = \begin{bmatrix} \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \sin\theta & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \begin{bmatrix} V_{Lq}^* \\ V_{Ld}^* \\ V_{L0}^* \end{bmatrix}. \quad (5)$$

ANFIS is a combined neuro-fuzzy system that uses the learning potential of neurons to FIS to provide an optimized Fuzzy Inference System (FIS). It uses a hybrid backpropagation algorithm for training neurons of each layer. The ANFIS architecture consists of a five-layer network, as shown in Fig. 5.

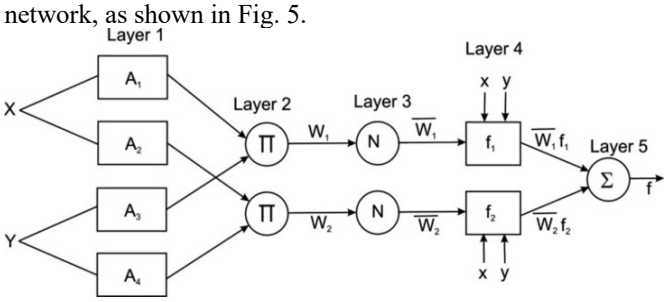


Fig. 5 – ANFIS controller-structure.

5. SIMULATION RESULTS

The test system is a three-phase 415 V, 50 Hz distribution grid and is connected with a 10 kVA linear load using a distribution line with impedance values R = 2.5 Ω, L = 3 mH. The maximum magnitude of the load voltage is 340V. This system creates 80 % sag voltage by adding three phases to the ground fault with a fault resistance of 0.85 Ω. Thus, the magnitude of the load voltage is reduced to 68V. The swell event of 150 % is created by adding 600 MVAr capacitive loads to the distribution system. Thus, the load voltage magnitude increases to 510 V from 0.15 s to 0.35 s.

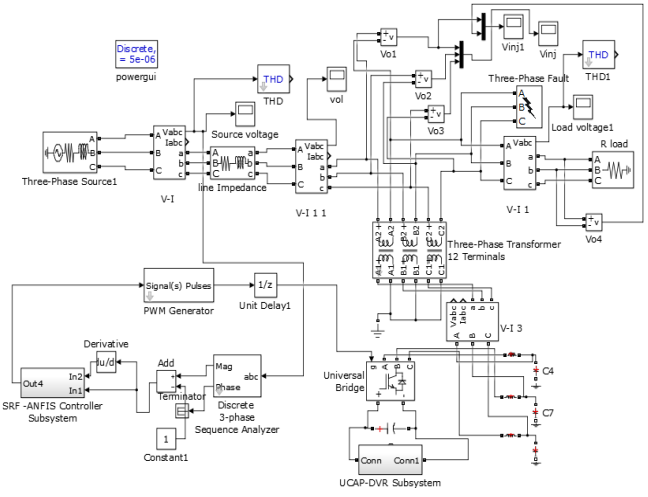


Fig.6 – UCAP-DVR integrated distribution system.

The proposed UCAP-DVR is interconnected with the distribution system using an SRF-ANFIS controller and tested for various % of both balanced and unbalanced sag and swell issues. The Simulink model of the UCAP-DVR interconnected distribution grid is shown in Fig. 6. UCAPs are used as the dc input source for DVR. The test system taken is the three-phase distribution system connected to the linear load.

DVR consists of VSI, which is added in series between the source and the load through the injection transformer. The reference voltages for the UCAP-DVR are calculated using the SRF ANFIS controller to enhance its compensation capability. During PQ problems, this DVR produces the required magnitude and phase angle of voltage added to the load voltage to improve the quality of load voltage even though there is a distortion in the supply voltage. The output side of VSI is connected in series with an injection transformer; the source side of VSI is linked to UCAP using a dc-dc converter to maintain the rigid dc-link input voltage for DVR.

The simulated structure of the SRF-ANFIS controller is exposed in Fig. 7. In this setup, two ANFIS controllers are used. One is for controlling the d component voltage error, and the second is for controlling the q component voltage error. The error signal is the error voltage obtained from the variation between the actual and reference load voltage.

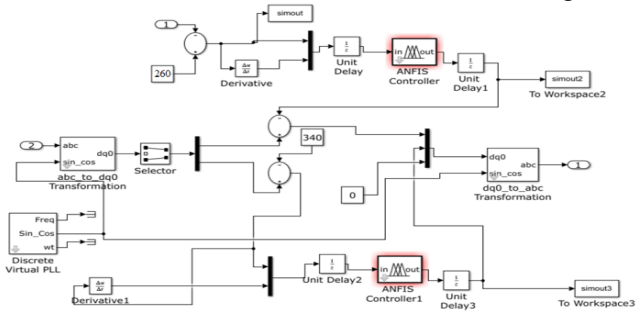


Fig. 7 – SRF-ANFIS controller Simulink model.

It is considered as one input, and the change in error in terms of voltage is considered a second input for the d-axis and q-axis components of the ANFIS controller. The ANFIS parameters are shown in Table 2.

Table 2

ANFIS parameters

Parameters	Values
No of nodes	27
No of the training data set	1000
No of the testing data set	100
No of the fuzzy rules	9
No of epochs	100

The input to another PI controller is the error between the reference dc voltage and the sensed dc voltage used to regulate the dc bus voltage of DVR. The resultant output is given as a PWM controller to generate gating pulses to a VSI to produce three phases of 50 Hz sinusoidal voltage at the load terminal. The switching frequency of the PWM controller is 10 kHz. DVR dc-link voltages 360 V. About 70 % of the obtained data set was used for training after scaling them to normalized values between 0 and 1. The hybrid backpropagation algorithm is used for FIS training with 100 epochs. The input variables for both d- axis and q-axis ANFIS controller were designed to have 3 membership functions, each of triangular structure characterizing each of them is represented in Fig. 8(a,b).

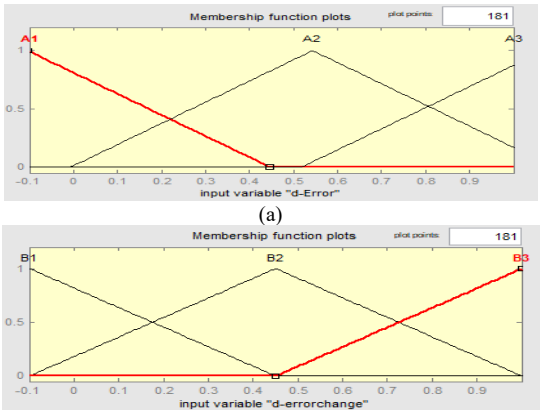


Fig. 8 – Membership function for ANFIS controller:
a. Error b. Change in error

A total of 1000 training data sets were obtained for various depths of voltage sag and swell by varying load impedance and fault resistance in the test system.

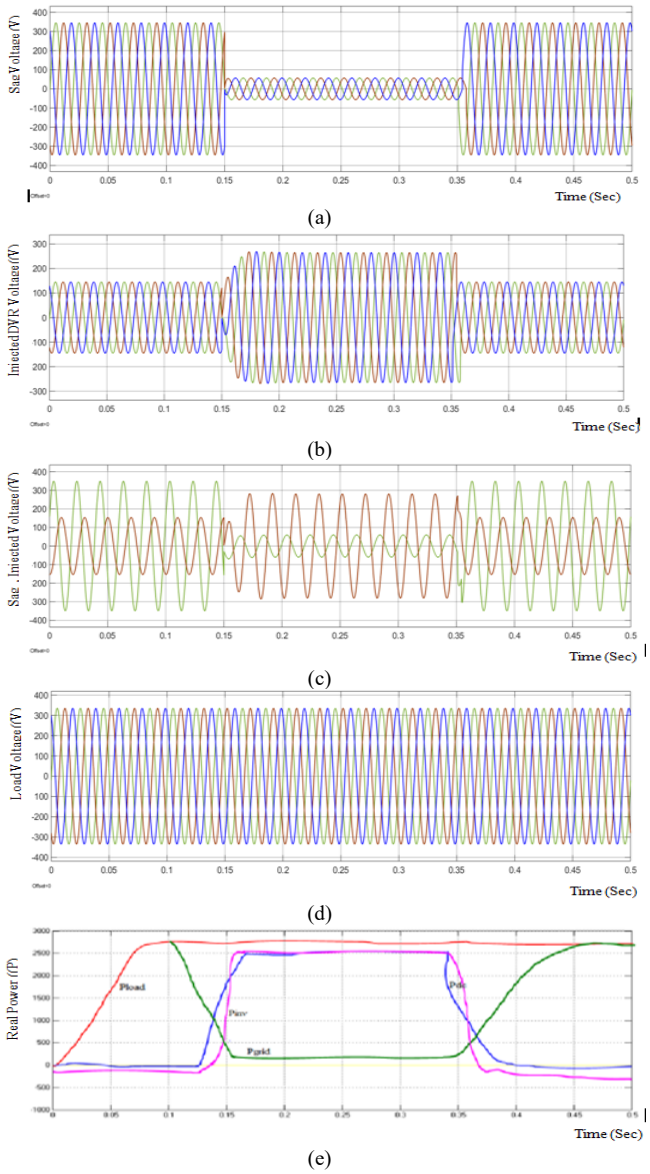


Fig. 9 – Simulation output of UCAP-DVR during sag: (a) sag voltage; (b) injected DVR voltage [V_{inja},V_{injb},V_{injc}]; (c) injected voltage V_{inja} (Red) & V_{0ab} (green); (d) load voltage; (e) real power output of load, inverter & grid.

The response of the UCAP-connected DVR during a sag event is depicted in Fig. 9 (a-c). The DVR injected voltage for all three phases (V_{inja},V_{injb},V_{injc}) is shown in Fig. 9 (b). A UCAP output voltage of 144 V is maintained during the normal period.

While the sag event is recognized, DVR affords the magnitude 128 V in all three phases to regulate the load voltage to the 340 V shown in Fig. 9 (c). The DVR injected voltage for phase A (V_{inja}) lags the source voltage (V_{0ab}) by 30º, which shows that the injected voltage is in the same phase as the line-neutral source voltage V_{0ab}. As a result, the load voltage is maintained at a constant value, as shown in Fig. 9(d). The real power output from the grid, load, inverter, and boost converter is shown in Fig. 9 (e). Figures 10 (a-c) show the UCAP-DVR's response to voltage swells' problems. During a swell event, the DVR injected voltage for all three phases (V_{inja},V_{injb},V_{injc}) is shown in Fig. 10 (a). From Fig. 10 (b), it is observed that the injected voltage V_{inja} lags V_{0ab} by 150º, which shows that it is out of phase with the 180º line-neutral voltage source V_{0ab}. Thus, the load voltage is regulated as constant. Thus, the voltage sag and swell problems are compensated effectively by the proposed UCAP-DVR in a precise and effective manner, as shown in Fig. 10 (c).

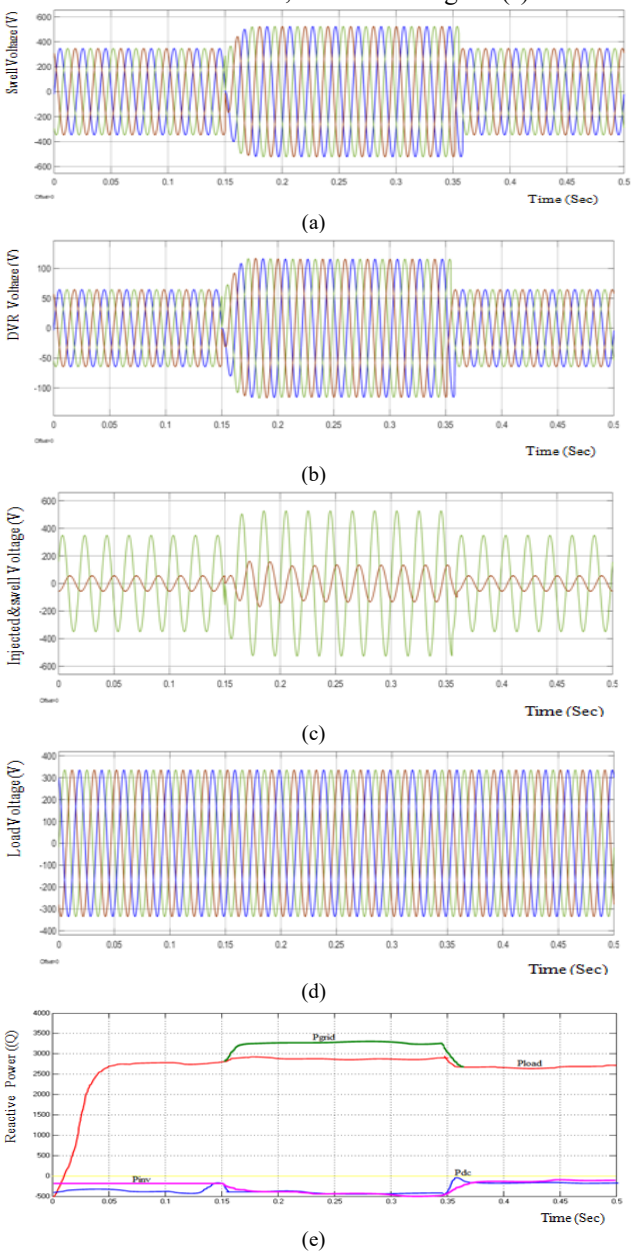
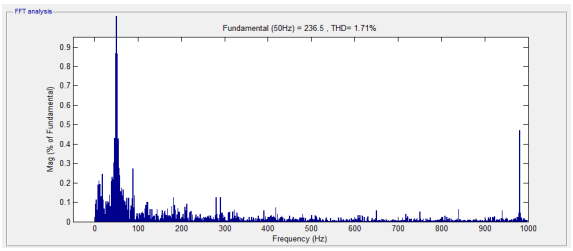
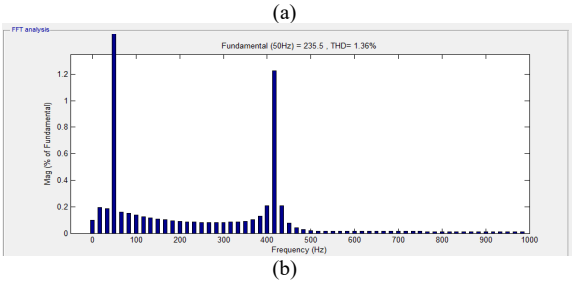


Fig. 10 – Simulation output of UCAP-DVR during swell: (a) swell voltage; (b) injected DVR voltage [V_{inja},V_{injb},V_{injc}]; (c) injected voltage V_{inja} (Red) and V_{0ab} (Green); (d) load voltage; (e) reactive power output of load, inverter & grid.

Figure 10 (e) depicts the real power output from the grid, load, inverter, and boost converter. From this, when a voltage swell happens, the power output from the grid (P_{grid}) increases, but the load maintains the output power P_{load} as almost constant. VSI absorbs the extra grid power. Now the dc-dc converter works in buck mode, so this power P_{inv} is stored in UCAP. The THD spectrum obtained for the compensated load voltage using the ANFIS controller is shown in Fig. 11 (a,b).



(a)



(b)

Fig. 11 – THD of load voltage after compensation: (a) sag; (b) swell.

The comparison of THD values for an uncompensated, UCAP-DVR with the PI controller, FUZZY controller, and the ANFIS controller for the voltage- related PQ issues sag and swell are shown in Table 3.

Table 3.

Performance comparison of controllers

System	THD for load voltage	
	Sag event	Swell event
Uncompensated	9.41 %	12.72 %
Integrated UCAP-DVR using the PI controller	5.71 %	7.71 %
Integrated UCAP-DVR using fuzzy controller	3.28 %	5.42 %
Integrated UCAP-DVR using ANFIS controller	**1.36 %**	**1.76 %**

This illustrates that the interconnected UCAP-DVR connected with the buck-boost converter using ANFIS controller affords a proficient and accurate compensation for the PQ issues voltage sag and swell and reduces THD of the source side voltage with the acceptable value.

6. HARDWARE IMPLEMENTATION

To validate the proposed UCAP-DVR topology experimentally, the hardware prototype of the single-phase UCAP-DVR was constructed and is shown in Fig. 12. The DVR model consists of MOSFET switches, their gate drivers, and an LC filter as explained in the converter. It also consists of an injection transformer with a 1:1 ratio. Here, two 18-0-18 V, 1 A transformers are used as injection transformers.

As the inverter is a line synchronized single-phase inverter, it requires a zero-crossing detector. The switching pulses required for inverter operation are generated using the PIC16F877A Microcontroller.

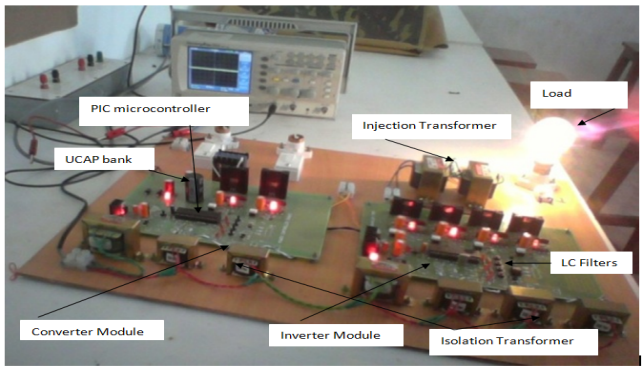


Fig. 12 – Hardware implementation of proposed DVR.

The hardware components used are shown in Table 4.

Table 4.

Hardware components Specifications

Components	Parameters
Inverter IGBT module	600 V, 100 A
Vdc dc-link capacitor	3500 µF, 300 Vdc
LC-filter	1.2 mH, 120 µF
Single-phase isolation transformers	2 kVA 125 /50 V
UCAP bank	Three 48 V, 165 F

The controller is programmed to produce a 10 kHz frequency. Here, the MCT2E Optocoupler IC drives the pulse to the switch. The generated gate pulse waveform for the inverter in the case where the grid experiences a voltage sag depth of 80 % and the inverter output voltage obtained is shown in Fig. 13. It can be observed that during the sag event, the DVR output voltage remains constant due to the injected voltage, which shows the ability of the proposed system.

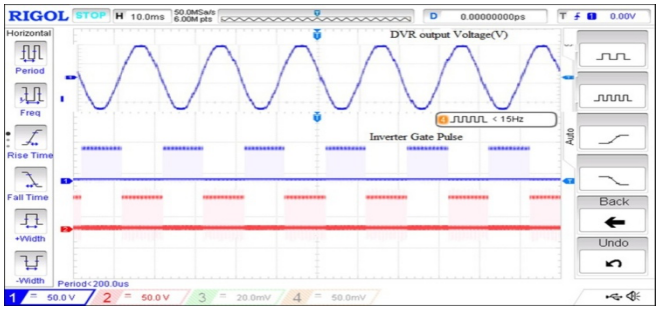


Fig. 13 – Inverter gate pulse, output voltage – experimental waveforms.

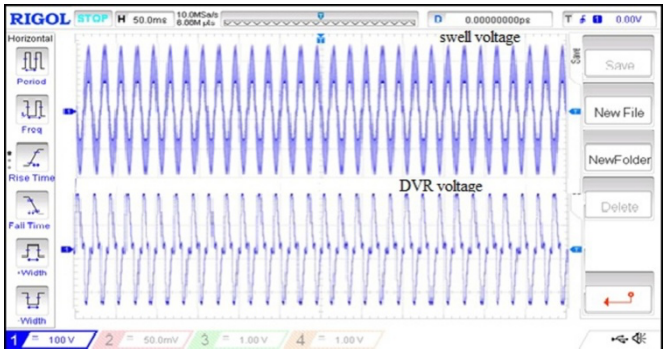


Fig. 14 – Swell event, DVR output voltage – experimental waveforms.

Therefore, from both inverter and dc–dc converter experimental waveforms, it can be concluded that the integrated UCAP-DVR system hardware setup can respond instantaneously to compensate for voltage sags. This proposed DVR is experimentally tested for the problem of voltage swell of depth 80 %, and the compensated output

voltage is shown in Fig. 14.

The power quality problem is thus mitigated when the DVR with a dc-dc converter is connected. The experimental hardware setup of the integrated system is presented, and the ability to provide temporary voltage sag and swell compensation in all three phases to the distribution grid dynamically is tested.

7. **CONCLUSION**

This paper exhibits the operation of DVR by introducing Ultracapacitor as a dc input voltage in DVR topologies for PQ enhancement in a three-phase distribution system. The bidirectional buck-boost dc-dc converter for integrating UCAP as a dc input for DVR was designed and modeled. Using an ANFIS controller, the UCAP-DVR has been established in a distribution grid for voltage-related problems. The results prove that this proposed UCAP can be used as an effective input source to DVR and maintain grid power even though the source is disturbed by PQ problems. It is proven that the integration of UCAP with DVR enhances the alleviating ability of DVR by maintaining its DC input voltage constant and affords active power support to the grid. This UCAP energy storage device increases a distribution grid's power consistency and energy protection. From the comparison results, it is inferred that the proposed ANFIS controller affords in-depth and proficient compensation for all kinds of PQ problems. This makes the proposed DVR topology more efficient and can be expanded to all PQ problems.

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