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PROPOSED POWER FACTOR CORRECTION CIRCUIT BASED ON THE SINGLE-ENDED PRIMARY-INDUCTOR CONVERTER CONTROLLED BY SLIDING MODE CONTROL STRATEGY USED IN AN ELECTRIC VEHICLE CHARGING STATION

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The quality of electrical energy has become a strategic issue for all economic actors. Its efficiency is reduced due to multiple disturbances and harmonic injections caused by the different connected loads. The electric vehicle (EV) takes an important place among these loads that take their energy from the grid through charging stations. In this paper, a solution to improve the power factor and reduce the harmonic injection is proposed by introducing a power factor correction (PFC) circuit in the charging stations. It is realized by a single-ended primary-inductor converter (SEPIC) that allows isolation between the load and the electrical network. In addition, it offers hardware minimization since it operates simultaneously in boost and buck without polarity reversal. A control technique based on the sliding mode control (SMC) technique is proposed for harmonic reduction and power factor correction. SMC is used to maintain the output voltage of the SEPIC converter at its desired value, improve the power factor (PF) and reduce the total harmonic distortion (THD). A software-in-the-loop (SIL) simulation using a real-time simulation platform (RT LAB) is performed to confirm the system's performance.

1. **INTRODUCTION**

The electric vehicle allows cleaner and more economical travel in terms of energy and maintenance thanks to its new traction mode, which is essentially composed of electric motors [1]. The source of electrical energy, which powers the traction motors, comes from the battery bank, and has the benefits of an electric vehicle with zero tailpipe emissions [2]. The recharge of these batteries is done through a recharging station composed of protection elements, control, and a set of power converters.

Dc-dc converters are the key elements of ac-dc-ac and dc-ac energy conversion systems. They are used in several applications such as domestic chargers, industrial power supplies, electric welding, and in electric vehicle battery charging. In this recently mentioned application, several topologies are developed and classified according to their degree of complexity. It is worth noticing that the topology classification scale is determined by the complexity degree of the mathematical modeling of the converter.

In numerous applications, ac-dc converters are inserted as an interface between the electrical networks and the dc-dc converters, as it is illustrated in Fig. 1.

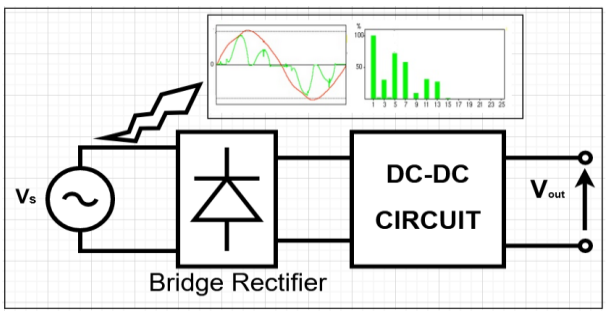

Fig. 1 – Ac-dc conversion system.

One can see from this figure how the presence of the converters affects the energy waveform quality of the network. This is mainly due to power electronic devices that induce undesired harmonics in the network, leading to an increase in the total harmonic distortion and then deterioration of the system power factor. To overcome the previously mentioned drawbacks, one of the best ways is the introduction of power factor correction circuits. Several passive and active power factor correction (PFC) schemes have been proposed [3,4]. However, passive correction is expensive, cumbersome, and used only for particular frequencies. Active PFC circuits are more flexible to be suitable for each different configuration.

Various active topologies are used, such as buck converter, boost converter, Cuk converter, and SEPIC converter. The buck converter used in [5,6] has the advantage of minimizing output voltage ripples, but the downside is that it provides an output voltage that is always lower than the input voltage. In [7–9], the boost converter is characterized by simplicity of control, it can provide an output voltage consistently high and has ripples in the output voltage. The Cuk converter combines the two advantages of buck and boosts output voltage except that it is reversed polarity as demonstrated in [10,11]. To overcome the disadvantages of the dc-dc converters mentioned above, we have chosen the SEPIC dc-dc converter for the PFC circuit. It offers some attractive advantages: it can provide an output voltage higher than the input voltage like the boost or lower like the buck without reversing polarity.

Furthermore, it provides isolation between the source side and the control side using the coupling capacitor. It has a high-power density compared to other converters. These advantages are put forward in several articles and among them that of reference [12], which discusses the battery charger.

In this paper, the SEPIC converter is used for active PFC and controlled by the sliding mode control technique (SMC), as shown in Fig. 2.

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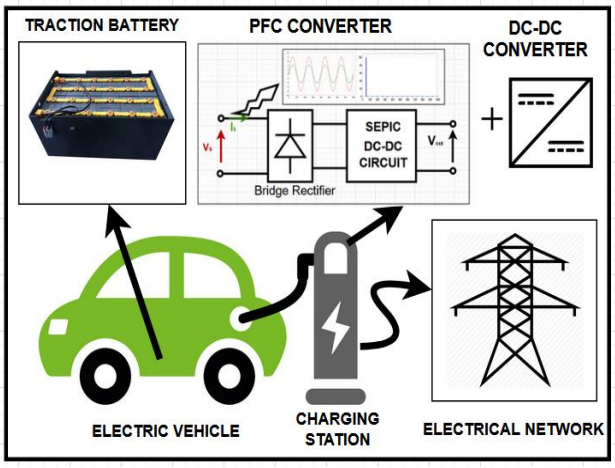

Fig. 2 – Global system scheme.

It performs multiple tasks such as active wave shaping of input current, high-frequency switching filtering, and feedback control to regulate the output voltage. A modification of the classic regulators by applying sliding mode is proposed. Then, a sliding mode observer is proposed to estimate the state vector and the load required to implement the control law. Details about sliding mode, such as vector control and attractiveness surface determination, are provided in section 3. System structure and dc-dc SEPIC state-space model are highlighted in section 2. Finally, the last section is dedicated to the presentation and the analysis of the experimental results and tests.

2. SYSTEM MODELING AND ARCHITECTURE

The proposed PFC system highlighted with dark dashed lines is made of two subsystems, as shown in Fig. 3.

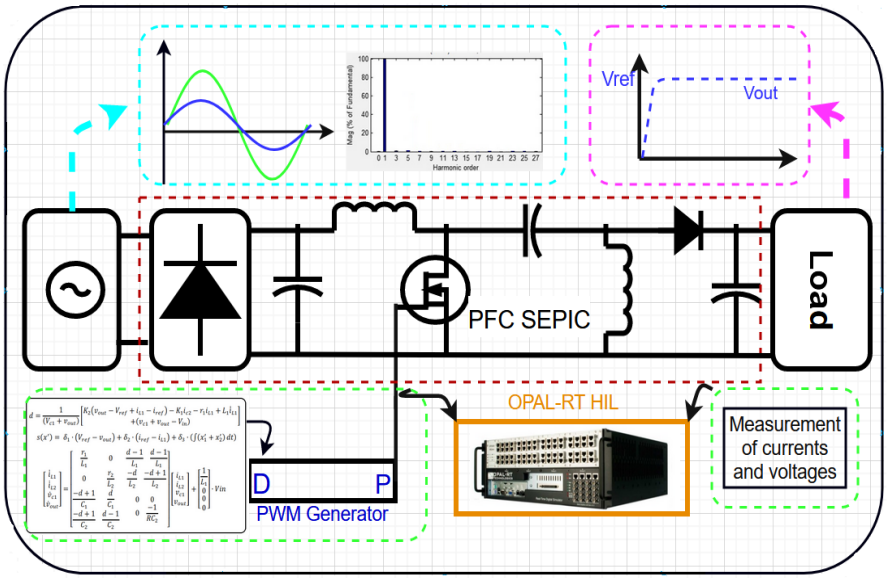

Fig. 3 – Proposed system architecture.

The first subsystem is a diode bridge used to rectify the ac input voltage to a dc voltage. The second subsystem is a SEPIC dc-dc circuit whose internal structure is detailed in Fig. 4, and it is controlled by the SMC technique.

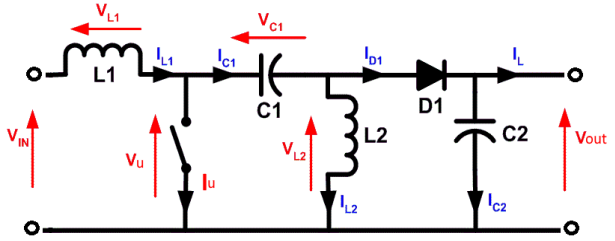

Fig. 4 – SEPIC internal structure.

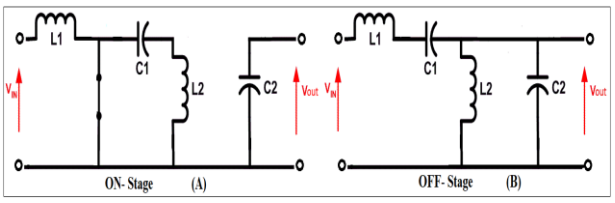

Fig. 5 – SEPIC converter operations.

The SEPIC converter is a four-order bilinear model whose state space representation depends on the state of the controlled switch u. Figure 5a shows the SEPIC circuit when the switch is closed (u = 1) and eq. (1) highlights its corresponding state space representation. Figure 5Sb mentions the SEPIC circuit when the switch is open (u = 0), and its dynamics are represented by eq. (2). It is worth noticing that the two equations mentioned above were derived assuming continuous conduction mode (CCM).

$$u=1\begin{cases}\dot{x}=A_1\cdot x+B_1\cdot V_{\text{in}}\\ y=\boldsymbol{C}_1^{\text{T}}\cdot x\end{cases}, \tag{1}$$

$$u=0\begin{cases}\dot{x}=A_2\cdot x+B_2\cdot V_{\text{in}}\\ y=\boldsymbol{C}_2^{\text{T}}\cdot x\end{cases}, \tag{2}$$

where x is a state variable given by eq. (3), is the current through inductance L_1, is the current through inductance L_2, is the voltage across the coupling capacitor C_1 terminals, and is the voltage across the bus capacitor C_2.

$$x=(i_{L1},i_{L2},V_{C1},V_{\text{out}})^{\text{T}}. \tag{3}$$

The coefficients of the matrices A_1, A_2, B_1, B_2, C_1, and C_2 are composed of circuit elements and load resistance. It is important to mention that the internal resistances of SEPIC inductances were considered during the analysis.

$$\begin{bmatrix} \dot{i}_{L1} \\ \dot{i}_{L2} \\ \dot{V}_{C1} \\ \dot{V}_{\text{out}} \end{bmatrix} = \begin{bmatrix} \frac{r_1}{L_1} & 0 & \frac{d-1}{L_1} & \frac{d-1}{L_1} \\ 0 & \frac{r_2}{L_2} & \frac{-d}{L_2} & \frac{-d+1}{L_2} \\ \frac{-d+1}{C_1} & \frac{d}{C_1} & 0 & 0 \\ \frac{-d+1}{C_2} & \frac{d-1}{C_2} & 0 & \frac{-1}{R\cdot C_2} \end{bmatrix} \cdot \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{\text{out}} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \cdot V_{\text{in}}, \quad (4)$$

where r_1 and r_2 are respectively the equivalent series resistances of inductances L_1 and L_2; d is the duty cycle which is a gain between 0 and 1.

3. **SLIDING MODE CONTROL**

Sliding mode control is a methodological approach to non-linear control used in many applications, especially for non-linear systems with various structures such as power converters. It consists of choosing a surface that represents the ideal characteristic, and once the state reaches this surface, the error regulation tends to zero as time goes to infinity [13]. Compared to other non-linear control strategies, this control strategy is distinguished by its simplicity of implementation compared to other control techniques and its robustness against external disturbances.

To synthesize the control vectors to be used, the following four requirements listed below must be simultaneously satisfied:

- Limit the number of parameters to be tuned;
- Stabilize SEPIC current;
- Maximize system power factor;
- Minimize THD percentage.

V_{out} and i_{L1} are chosen as control variables to determine the sliding surface, which is of the type given in

$$s(x') = K^{\text{T}} \cdot x', \quad (5)$$

where s is the sliding surface, K is a gain matrix and x' is the control vector to be synthesized. The chosen control vector is expressed in

$$x' = \begin{bmatrix} x_1' \\ x_2' \\ x_3' \end{bmatrix} = \begin{bmatrix} v_{ref} - v_{out} \\ i_{ref} - i_{L1} \\ \int (x_1' + x_2')\text{d}t \end{bmatrix}, \quad (6)$$

with

$$K^{\text{T}} = \begin{bmatrix} \delta_1 & \delta_2 & \delta_3 \end{bmatrix}. \quad (7)$$

Substituting with (6) and (7) in (5) and after-term expansion yields:

$$\begin{aligned} s(x') = \delta_1 \cdot \left(v_{\text{ref}} - v_{\text{out}}\right) + \delta_2 \cdot \left(i_{\text{ref}} - i_{\text{L1}}\right) + \\ + \delta_3 \cdot \left(\int (x_1' + x_2')\text{d}t\right), \end{aligned} \quad (8)$$

with V_{ref} and i_{ref} being the reference output voltage and inductance current, respectively.

Setting $\dot{s}(x') = 0$ and using eqs. (4) and (8), the relation between the SEPIC parameters defined previously, and the control vector can be obtained as illustrated by eq. (9).

$$\begin{aligned} \dot{x}_1' &= \frac{\text{d}}{\text{d}t}(V_{\text{ref}} - V_{\text{out}}) = \frac{-i_{C2}}{C_2}, \\ \dot{x}_2' &= \frac{\text{d}}{\text{d}t}(i_{\text{ref}} - i_{\text{L1}}) = \\ &= \dot{i}_{\text{ref}} - \frac{r_1}{L_1} i_{L1} - \frac{d-1}{L_1}(V_{C1} + V_{\text{out}}) - \frac{1}{L_1} V_{\text{in}} \\ \dot{x}_3' &= V_{\text{ref}} - V_{\text{out}} + i_{\text{ref}} - i_{\text{L1}}. \end{aligned} \quad (9)$$

Substituting $\dot{x}_1'$, $\dot{x}_2'$ and $\dot{x}_3'$ by their corresponding mathematical expressions given in eq. (9), and solving for duty cycle d, yields

$$\begin{aligned} d = & \frac{1}{(V_{C1} + V_{\text{out}})} \cdot \\ & \cdot \begin{bmatrix} (V_{C1} + V_{\text{out}} - V_{\text{in}}) - \frac{\delta_1 \cdot L_1}{\delta_2 \cdot C_2} \cdot i_{C2} + L_1 \cdot \dot{i}_{\text{ref}} \\ -r_1 \cdot i_{L1} + \frac{\delta_3 \cdot L_1}{\delta_2} \cdot (V_{\text{ref}} - V_{\text{out}} + i_{\text{ref}} - i_{L1}) \end{bmatrix}. \end{aligned} \quad (10)$$

For simplification reasons, we set:

$$K_1 = \frac{\delta_1 \cdot L_1}{\delta_2 \cdot C_2} \text{ and } K_2 = \frac{\delta_3 \cdot L_1}{\delta_2},$$

then eq. (11) becomes:

$$\begin{aligned} d = & \frac{1}{(V_{C1} + V_{\text{out}})} \cdot \\ & \cdot \begin{bmatrix} (V_{C1} + V_{\text{out}} - V_{\text{in}}) - K_1 \cdot i_{C2} + L_1 \cdot \dot{i}_{\text{ref}} \\ -r_1 . i_{L1} + K_2 \cdot (V_{\text{ref}} - V_{\text{out}} + i_{\text{ref}} - i_{L1}) \end{bmatrix} \cdot \end{aligned} \quad (11)$$

Attraction regions imposed by the SMC strategy can be determined using the relationship of the attractiveness condition $s\dot{s} < 0$. So, to ensure stability over the whole area of operation, the following inequalities are used for this purpose.

$$\begin{cases} \lim\limits_{\substack{s \to 0^- \\ d \to 0}} (\dot{s}) > 0, \\ \lim\limits_{\substack{s \to 0^+ \\ d \to 1}} (\dot{s}) < 0. \end{cases} \quad (12)$$

To ensure the attractiveness of the trajectory on the sliding surface over the entire operating range of the system and given the different design constraints already set, the following equations are obtained:

$$\begin{cases} V_{\text{in,max}} - K_2(V_{\text{ref}} - V_{\text{out}} + i_{\text{ref}} - i_{L1}) + K_1 \cdot i_{C2\text{max}} + \\ \quad + r_1 \cdot i_{L1\text{min}} - L_1 \cdot \dot{i}_{\text{ref\_min}} < (V_{C1\text{min}} + V_{\text{out}}) \\ V_{\text{in,min}} - K_2(V_{\text{ref}} - V_{\text{out}} + i_{\text{ref}} - i_{L1}) + K_1 \cdot i_{C2\text{min}} + \\ \quad + r_1 \cdot i_{L1\text{max}} - L_1 \cdot \dot{i}_{\text{ref\_max}} > 0. \end{cases} \quad (13)$$

$(K_1, K_2) = (0.03, 0.35)$ is a compromise solution for the inequality system shown in the equation above.

4. RESULTS AND DISCUSSION

To verify and analyze the nonlinear system previously mentioned, simulations under the MATLAB-Simulink environment were carried out. To confirm the obtained simulation results, a SIL simulation was performed using an RT LAB simulator. The basic architecture of any RT LAB-based simulation is highlighted in Fig. 6. The developed test bench using the RT LAB simulator is shown in Fig. 7. advanced real-time electromagnetic solvers (ARTEMIS) were used to build the model. ARTEMIS solves electrical systems using the state-space approach.

However, it precomputes and discretizes all State-Space matrices, for all combinations of switch topologies, before the real-time execution and stores them into the cache memory. The established model is divided into two subsystems: the console and the master. The parameters of the developed model are detailed in Table 1.

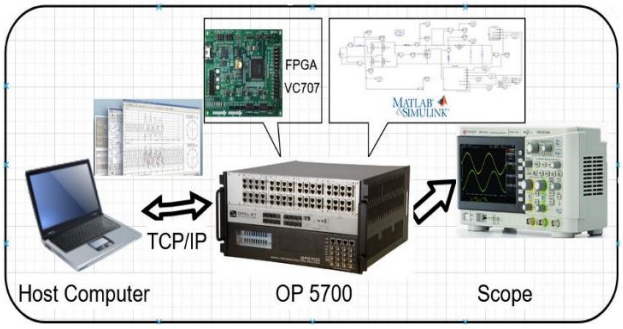

Fig. 6 – RT-LAB SIL system of the developed platform.

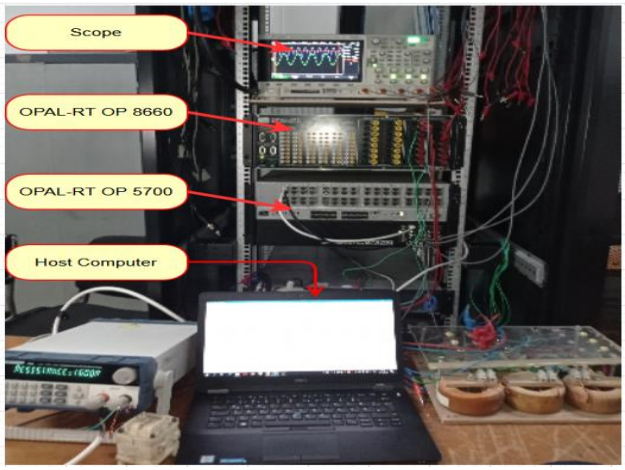

Fig. 7 – RT LAB-based test bench.

Table 1

Model parameters

Parameters	Values	Parameters	Values
V_{sline}	230·sqrt(2) V	r_1	0.01 Ω
V_{ref}	400 V	L_2	0.185 mH
f	50 Hz	C_1	2.435μF
f_{ws}	70 kHz	C_2	4000 μF
L_1	1.855 mH	R_{load}	26 Ω

The green plot shown in Fig. 8 represents the network line current. The red and blue color waveforms on the same figure highlight, respectively, the inductance current and its desired reference with an offset of 20 A. The three last-mentioned currents are synchronized, and all have the same frequency. The obtained simulation results shown in Fig. 8a are by the SIL simulation results shown in Fig. 8b.

The second controlled variable is V_{C2} or V_{out}. Its plot is shown in Fig. 9. Again, one can state a perfect match between the simulation and the implementation results. It can be seen that follows its reference set to 405 V with tolerable voltage fluctuations, which lie within an imposed narrow band. From the measurement window shown in Fig. 9b it can be deduced that the voltage fluctuation is about 10 % of the nominal dc bus voltage.

Figure 10 represents the network current and voltage, the input to the rectifier circuit. Both current and voltage are in phase, which increases the system power factor. From the measurement window shown in Fig. 10,b, it can be seen that the shift angle between network current and voltage is very small and equal to φ = 0.9°, which results in a power factor close to unity PF = cos(φ) = 0.999.

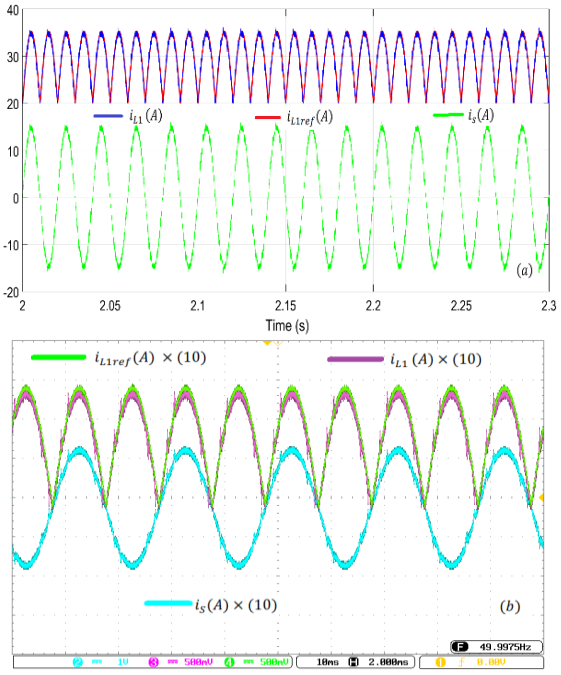

Fig. 8 – Current synchronization: a) MATLAB simulation; b) real-time hardware implementation.

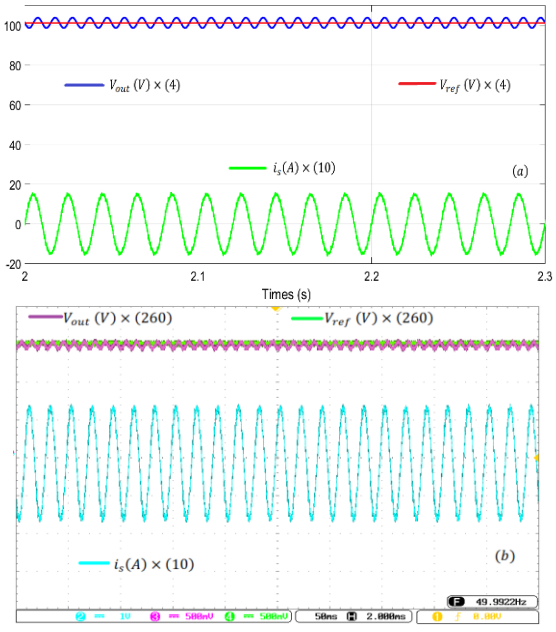

Fig. 9 – Dc bus: a) MATLAB simulation; b) real-time hardware implementation.

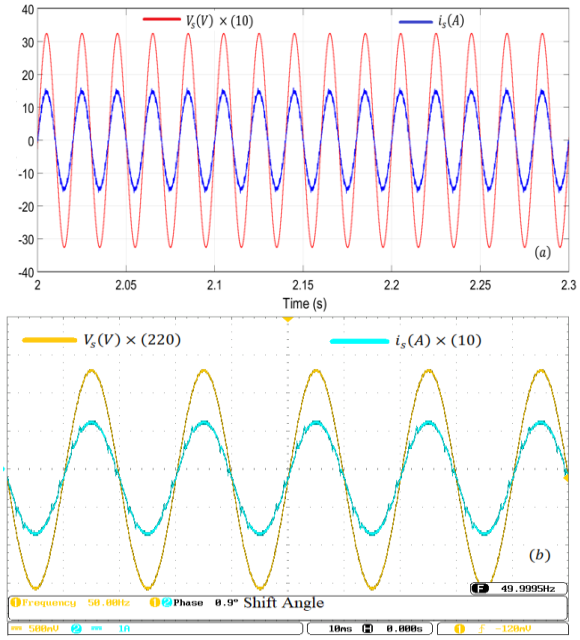

Fig. 10 – Rectifier input current and voltage: a) MATLAB simulation; b) real-time hardware implementation.

Figure 11 represents a zoom of the network current along with its FFT frequency analysis. It could be seen that the control technique resulted in smoothening the current shape and reducing its THD, as shown in Fig. 11. From Fig. 11b, it could be deduced that the THD is equal to 4 %, which is a very satisfactory and acceptable harmonic ratio according to IEC 61000-3-2 and IEEE 519 standards.

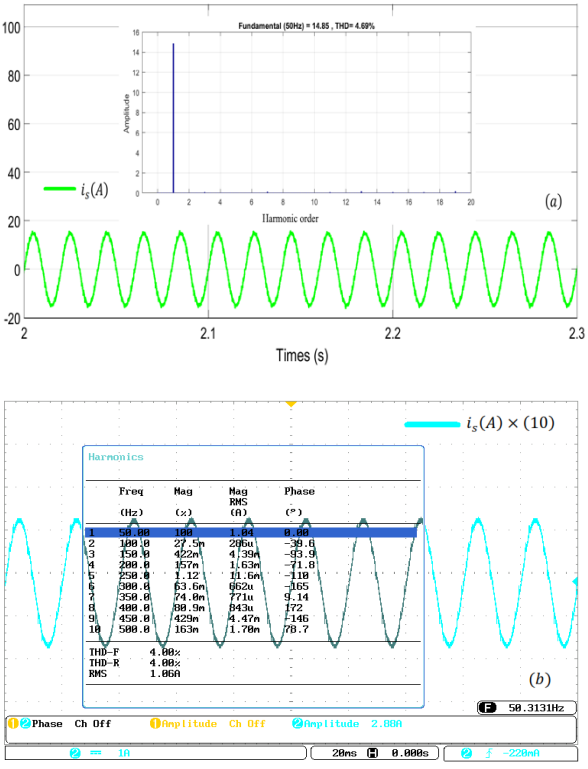

Fig. 11 – Line current and frequency analysis: a) MATLAB simulation; b) real-time hardware implementation.

5. CONCLUSION

In this article, we have presented a PFC circuit model based on the SEPIC converter controlled by the second order sliding mode control (SMC) technique used in electric vehicle charging stations. SIL validation of the proposed control technique using the RT LAB simulation platform is performed to verify the results obtained. The SMC control technology demonstrates good performance and compromise between simplicity and efficiency. Significant THD reduction and power factor improvement was observed after applying the proposed SMC technique to the SEPIC converter.

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REFERENCES

1. D. Ziane, S. Aissou, A. Azib, T. Rekioua, *Performance test of the control strategy applied to the electric vehicle, in the case of FWD and 4WD*, Int J Hydrogen Energy, **39**, pp. 21259-21264 (2014).
2. A. Azib, D. Ziane, T. Rekioua, *Ensure continuity of operation of an electric vehicle under fault condition in converter*, International Journal of Hydrogen Energy, **41**, pp. 9066-9074 (2016).
3. S. Aiswariya, R. Dhanasekaran, *Simulation and analysis of a single-phase ac-dc boost PFC converter with a passive snubber for power quality improvement*, IEEE International Conference on Advanced Communication Control and Computing Technologies, 2014.
4. K.I. Hwu, C.-L. Tsai, K.-F. Lin, *A simple passive ZCS circuit for PFC converter*, 23rd Annual IEEE Applied Power Electronics Conference and Exposition, 2008.
5. D.D.C Lu, S.K Ki, *Light-load efficiency improvement in buck-derived single-stage single-switch PFC converters*, IEEE Transactions on Power Electronics, **28**, *5*, pp. 2105 – 2110 (2013).
6. S. Singh, B. Singh, *PFC buck converter fed PMBLDCM drive for low power applications*, IEEE Fifth Power India Conference, 2012.
7. R.J. Ganesh, S. Kodeeswaran, M. Kavitha, T. Ramkumar, *Performance analysis of piezoelectric energy harvesting system employing bridgeless power factor correction boost rectifier*, Materials Today: Proceeding, **45**, *25*, pp. 486-494 (2021).
8. P.R. Mohanty, A.K. Panda, Dh. Das, *An active PFC boost converter topology for power factor correction*, Annual IEEE India Conference (INDICON), 2015.
9. O. Turksoy, U. Yilmaz, A. Teke, *Efficient ac-dc power factor corrected boost converter design for battery charger in electric vehicles*, Energy, **221**, pp. 119765 (2021).
10. S. Ketsingsoi and Y. Kumsuwan, *An off-line battery charger based on buck-boost power factor correction converter for plug-in electric vehicles*, 11th Eco-Energy and Materials Science and Engineering (11th EMSES), Energy Procedia, **56**, pp. 659– 666 (2014).
11. B. Wang, J. Xu, D. Xu, Z. Yan, *Implementation of an estimator-based adaptive sliding mode control strategy for a boost converter-based battery/supercapacitor hybrid energy storage system in electric vehicles*, Energy Conversion and Management, **151**, pp. 562-572 (2017).
12. B. Anton, A. Florescu, S. G. Rosu, *Standalone analog active cell-balancing circuit for automotive battery management systems*, Rev. Roum. Sci. Techn.– Électrotechn. et Énerg,, **63**, *3*, pp. 306–313 (2018).
13. A. Mourad, G. Keltoum, *Power system stabilizer based on terminal sliding mode control*, Rev. Roum. Sci. Techn.– Électrotechn. et Énerg., **62**, *1*, pp. 98–102 (2017).
14. V. Subramanian, S. Manimaran, *Implementation of a sliding mode controller for single ended primary inductor converter*, Journal of Power Electronics, **15**, *1*, pp. 39-53 (2015).
15. O.L. Santo *et al.*, *Sliding mode control of the isolated bridgeless SEPIC High Power Factor Rectifier Interfacing an AC Source with a LVDC Distribution Bus*, Energies, **12**, p. 3463 (2019).
16. S. Ma *et al.*, A *Sliding mode control method for sepic power factor correction converter*, IPEMC2020-ECCE, Asia.