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ZERO-VOLTAGE SWITCHING SOLUTIONS IN SINGLE-ENDED FORWARD TOPOLOGIES OVER ANY OPERATING CONDITIONS

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Keywords: Single ended forward topology; Zero-voltage switching; Single-ended forward with active clamp; Two transistors forward.

In this paper, a novel solution is presented to enable zero-voltage switching (ZVS) under any operating condition, utilizing transformers with extremely low leakage inductance. The proposed methods ensure that the primary switches turn on at zero voltage while the secondary rectifiers turn off at zero current. While numerous ZVS techniques for single-ended forward topologies have been proposed over the years, most rely on transformer leakage inductance to delay the current flow to the secondary. Although these approaches achieve zero-voltage switching (ZVS) for the primary switches, they fail to achieve zero-current switching (ZCS) in the secondary rectifiers. Additionally, a larger leakage inductance reduces the effective duty cycle, often necessitating a turns ratio adjustment to maintain regulation at the minimum input voltage. This adjustment increases the primary RMS current and higher voltage stress in the secondary. In contrast, this paper presents a ZVS solution specifically designed for forward converters with low leakage inductance, making it particularly suitable for wide input voltage ranges, high-current applications, and high-frequency operation.

1. INTRODUCTION

Since the early 1990s engineers investigated developing solutions ~~in~~ to convert~~ing~~ hard switching topologies such as forward converters ~~into~~ in soft switching topologies. ~~due to t~~The continuous demand for miniaturization required higher frequency of operation. As a result of higher frequency ZVS became a necessity to reduce the switching losses and increase the efficiency. Most topologies in power converters in medium and high-power applications are forward derived topologies. Half bridge and full bridge topologies for example are forward derived topologies. In many medium power applications single ended forward topology ~~became~~ is very popular. Two of such topologies are two transistors forward and single ended active clamp topology. Single ended forward topology with active clamp became very popular due to its ability to obtain ZVS in certain conditions. That was because by controlling the amplitude of the magnetizing current and with appropriate leakage inductance zero voltage switching could be accomplished. The conventional wire wound transformers used in the industry have a coupling coefficient in the range of K = 0.992-0.996.

$$L_{lk} = L_P(1 - K^2), \qquad (1)$$

where L_{lk} is the leakage inductance in the transformer, L_p is the inductance of the primary winding and K is the coupling coefficient between primary and secondary winding.

Using formula (1) results that the leakage inductance reflected in the primary is in between 2uH to 5uH, for a primary inductance of 300uH. In addition to that I may have to add also the effect of the stray inductance, which will further increase the effective leakage inductance. In the last 30 years, the introduction of planar magnetics and the large utilization of SMD devices, the stray and the leakage inductance has been decreased substantially in many applications. For leakage inductance in between 2uH-5uH and using a large magnetizing current ZVS across the primary switchers can be obtained, especially at full load. For very low leakage inductance magnetics wherein K> 0.998, which means leakage inductance less than 1uH, ZVS, cannot be obtained by using very large magnetizing current ~~solutions~~. In Fig. 1 is depicted a single ended forward topology using active clamp.

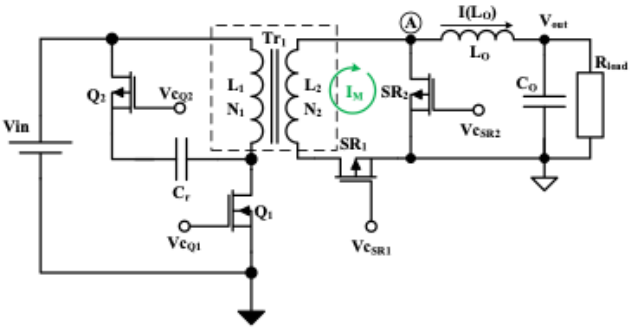

Fig. 1 – Single ended forward with active clamp [1]

In Fig. 2 the key waveforms are presented. The key waveforms are: control signals for the switch Q_1 and Q_2, the current through the clamp capacitor, C_r, the current through the main power switch Q_1, the voltage across the main power switch $V_{ds(Q1)}$, and the magnetizing current I_M. The magnetizing current is calculated based on formula (2).

$$I_M = N_1 * I(L_1) + N_2 * I(L_2), \qquad (2)$$

where I_M is the magnetizing current, N_1 is the number of turns in the primary winding, $I(L_1)$ is the current through the primary winding, N_2 is the number of turns in the secondary winding and $I(L_2)$ is the current through the secondary winding.

There are five time intervals that are presented below:

Interval 1 [t_0 to t_1] the main power switch Q_1 is on and the current is flowing through the primary of the transformer T_{r1}, as depicted by $I_{d(Q1)}$. The magnetizing current I_M is building up its amplitude during this time interval.

At t_1 the main power switch is turned off and the current flowing through the leakage inductance L_{lk} will continue to flow for the time interval 2 [t_1 to t_2].

Interval 3 [t_2 to t_3] magnetizing current will flow via the clamp capacitor C_r and will reach zero at t_3. Further the magnetizing current is mirrored back into the negative region in the interval 4 [t_3 to t_4].

Interval 5 [t_3 to t_4]. At t_4 the current through C_r has the amplitude of the magnetizing current I_M at t_1 but of negative polarity.

The clamp switch Q_2 is turned off at t_4 and the magnetizing current will flow via the parasitic capacitance of Q_1 from source towards the drain. The voltage across Q_1 will

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discharge from $V_{in}/(1-D)$ to a voltage level equal to V_{in} at t_4. At t_4 the SR_2 is conducting the current through L_o. For a negligeable value of the leakage inductance, which means a very high coupling coefficient $K > 0.998$ the secondary circuit formed by SR_2 and the body diode of SR_1 will act as a short circuit and the magnetizing current I_M is maintaining the same amplitude.

The secondary short circuit in between t_4 to t_5 does not allow the magnetizing current I_M to transfer to the primary side to further discharge the parasitic capacitance reflected across Q_1 and ZVS cannot be obtained.

In summary, the secondary-side short circuit formed by SR_2 and the body diode of SR_1 maintains a constant magnetizing current and prevents the complete discharge of Q_1's parasitic capacitance. This behavior is inherent in forward-derived topologies with extremely low leakage inductance, making zero-voltage switching (ZVS) unattainable in such configurations.

In all the forward-derived topologies, the short circuit formed in the secondary by the conduction of SR_2 and SR_1 prevents obtaining ZVS in applications with negligible leakage inductance between the primary and secondary.

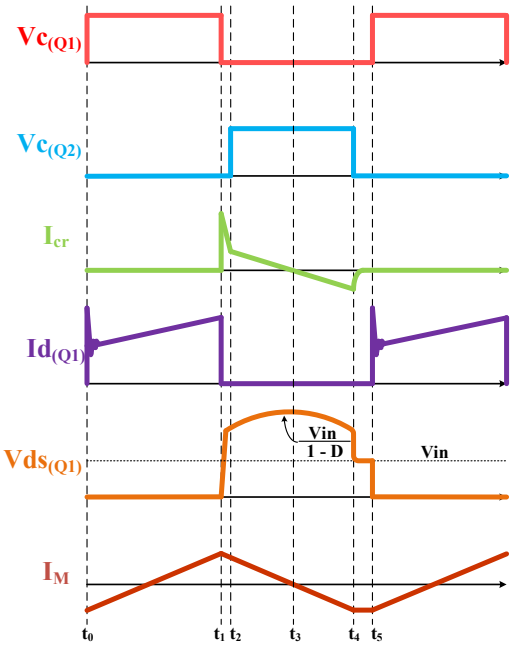

Fig. 2 –The key waveforms of the circuit from Fig. 1 [1].

A solution to overcome this problem was presented in the reference [2], using a nonlinear magnetic element in the secondary in series with the forward rectifier. This solution, however, will create hysteresis losses in the nonlinear magnetic core element.

In this paper, I will present a solution that enables ZVS under any operating condition using a transformer with minimal leakage inductance.

2. DETAILED ANALYSIS OF THE TWO TRANSISTORS FORWARD TOPOLOGY

In Fig. 3, the basic schematic of the single-ended, two-transistor forward topology is presented. It is formed by two primary switching devices M_1 and M_2 which are turned on and off at the same time, two reset diodes D_{R1} and D_{R2}, which have several functions. One function is to reset the transformer T_{r1} by placing the primary winding across the input voltage V_{in}, with the opposite polarity to the existing polarity during the conduction of M_1 and M_2. In addition to the function of resetting the transformer core, the D_{R1} and D_{R2} create a path for the leakage inductance to transfer its energy to the primary input voltage source. In the secondary there are two rectifiers SR_1 and SR_2 and the output filter formed by L_o and C_o.

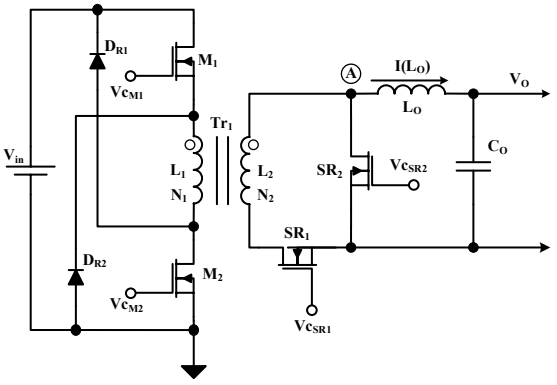

Fig. 3 – Two transistors forward with Synchronous rectifiers [3]

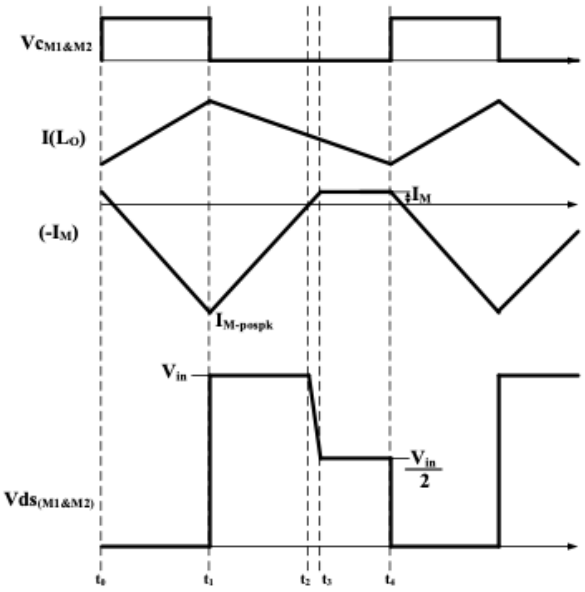

Fig. 4 – The key waveforms of the circuit from Fig. 3 [3].

The key waveforms of this topology are presented in Fig. 4. The key waveforms are: $V_{cM1\&M2}$, the control signal for M_1 and M_2, $I(L_o)$ which represents the current through the output inductor L_o, I_M which represents the magnetizing current in the transformer T_{r1}, and $V_{ds(M1\&M2)}$, which means the voltage across M_1 and M_2.

From Fig. 4, four intervals are identified as follows.

Interval 1 [t_0 to t_1]: the main primary switches M_1 and M_2 are on, and during this time, the current through L_o increases, wherein energy is stored in L_o and some energy is transferred to the secondary towards C_o and R_{load}. During the conduction of M_1 and M_2, the magnetizing current in the transformer increased between t_0 to t_1. The magnetizing current is presented in Fig. 4 multiplied by (-1), as ($-I_M$). The purpose of this inversion is to make a visual comparison between the current through the output inductor $I(L_0)$ and ($-I_M$) as depicted in Fig. 4.

Interval 2 [t_1 to t_2] is the reset period of the transformer T_{r1}, and the magnetizing current ($-I_M$) reaches zero at t_2.

Interval 3 [t_2 to t_3]. Between t_2 and t_3, the voltage across M_1 and M_2 starts decaying from an amplitude of V_{in} to an amplitude of $V_{in}/2$. Figure 5 presents the voltage across the switching elements M_1 and M_2 during this transition, as well as the magnetizing current during the same transition from the V_{in} to $V_{in}/2$ section, which is shaded. The difference in the energy contained in the parasitic capacitances before and after the transition is converted into magnetizing current energy, defined by I_M.

Interval 4 [t_3 to t_4]: Between t_3 and t_4 is the dead time wherein no energy is processed.

The negative component of the magnetizing current flows into the secondary as depicted in Fig. 1, flowing into the node A, while the output current $I(L_o)$ flows from the point A towards L_o and the output. By depicting the ($-I_M$) rather than (I_M), we get a visual representation of the currents going in and out of the switching node A. The negative portion of the magnetizing current goes into the switching node A, flowing from the secondary winding L_2, and the current through L_o flows out of the switching node A for a positive polarity of the current through L_o.

I will introduce the terminology of a "positive" magnetizing current I_M-poz, magnetizing current which is increasing during the conduction of the main primary switchers M_1 and M_2 and a "negative" magnetizing current I_M-neg whose absolute amplitude decreases during the conduction of D_{R1} and D_{R2}.

Between t_1 to t_2, the reset diodes DR_1 and DR_2 conduct the magnetizing current is resetting the transformer Tr_1, and in process the magnetizing current decreases its amplitude from I_M-neg-pk at t1 to zero at t_2.

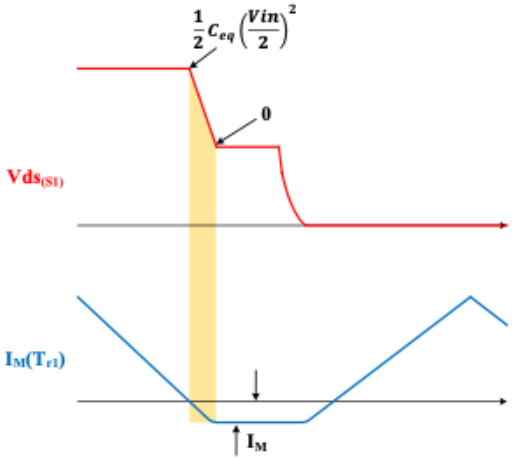

Fig. 5 – Upper trace: voltage across M_1 and M_2 from Fig. 3. Lower trace: current through primary winding of T_{r1} from Fig. 3.

In Fig. 5 is depicted the voltage across the primary switching elements and the magnetizing current through the transformer. As can be seen when the voltage across the primary switching elements decays from the V_{in} level to $V_{in}/2$ level, visualized by the shaded area, and the magnetizing current becomes negative. The negative value of the magnetizing current represents the energy obtained from the energy of the parasitic capacitance across the switching elements decaying from V_{in} to $V_{in}/2$. The negative magnetizing current I_M amplitude can be derived from:

$$I_M = (N * V_O) / \sqrt{\frac{L_1}{C_{eq}}}, \quad (3)$$

where I_M is the magnetizing current, N is the turns ratio in the transformer , L_1 is the inductance of the primary winding of the transformer and C_{eq} is the parasitic capacitance reflected across the primary switching elements.

The negative magnetizing current is proportional with the input voltage, and the primary inductance and equivalent parasitic capacitance C_{eq} which is defined by the formula (4) which means that the equivalent parasitic capacitance is the summation of the parasitic capacitance across each primary switching device and the parasitic capacitance reflected across the primary winding.

$$C_{eq} = C_{oss(M_1)} + C_{oss(M_2)} + C_{Trp}, \quad (4)$$

where $C_{oss(M1)}$ and $C_{oss(M2)}$ is the parasitic capacitance across M_1 and M_2 and C_{Trp} is the parasitic capacitance reflected across the primary of the transformer Tr_1

Between t_2 and t_3 the energy contained in the parasitic capacitance across the switching elements in the primary is converted in the magnetizing energy.

Between t_3 and t_4 the magnetizing inductance is shortened in the secondary side by the conduction of SR_2, which conducts the current through the output inductor, $I(L_o)$ and the body diode conduction of SR_1. The secondary short circuit previously described is also the reason that zero voltage switching cannot be obtained using the magnetizing current in applications with very low leakage inductance.

3. ZVS IN TWO TRANSISTORS FORWARD TOPOLOGY BY EMPLOYING THE NEGATIVE MAGNETIZING CURRENT

In Fig. 6 are presented the key waveforms in the single ended two transistor topologies depicted in Fig. 3, operating at different loading conditions.

At lighter loads the output current through L_o will have a lower amplitude and the min current through L_o, $I(L_o)_{Min}$ will reach the amplitude of $I_{M\text{-}neg}$ at t_3'. That will change the mode of operation after t_3'. At t_3' the magnetizing current flowing from the secondary winding into the switching node A will have the same amplitude as the current through Lo. That means that the current demanded by L_o will be fully provided by $I_{M\text{-}neg}$ and the current through SR_2 will become zero. Once the current through SR_2 will be zero the SR_2 can be turned off. That will open the secondary short circuit as previously presented. After t_3' once the current through L_o decreases, the extra current of I_M-neg will flow back into the primary and it will start discharging the parasitic capacitances across M_1 and M_2.

The voltage waveform in Fig. 6 clearly shows this discharge process – after t_3', the voltage across the switches decays in a resonant manner due to energy transfer from both the leakage inductance and the returning magnetizing current. This resonant discharge reduces the switch voltage by an amount ΔV_r during the initial phase.

After that there are presented 3 curves, #1, #2 and #3 which represents the discharge of the parasitic capacitances across M_1 and M_2 by the magnetizing current which is transferred back into the primary side. The voltage decay of the parasitic capacitance across M_1 and M_2 is function of the difference in between the magnetizing current reflected into the secondary and the current through output inductor. The current difference between the magnetizing current reflected in the secondary and the current through the output inductor, will reflect into the primary side and discharge the parasitic capacitance across M_1 and M_2. In the case of curve #3 the difference in between the magnetizing current reflected into

the secondary and the current through L_o is relatively small while in the case of curve #1 there is a larger current difference which is reflected into the primary and discharge the parasitic capacitances to zero at t_4. This method works in applications wherein I_M-neg which is presented in eq. (3) is larger than the minimum current through the output inductor. This method of obtaining ZVS in two transistors forward is presented in detail in [3]. To obtain ZVS at higher loads the current injection method can be used as described in [4].

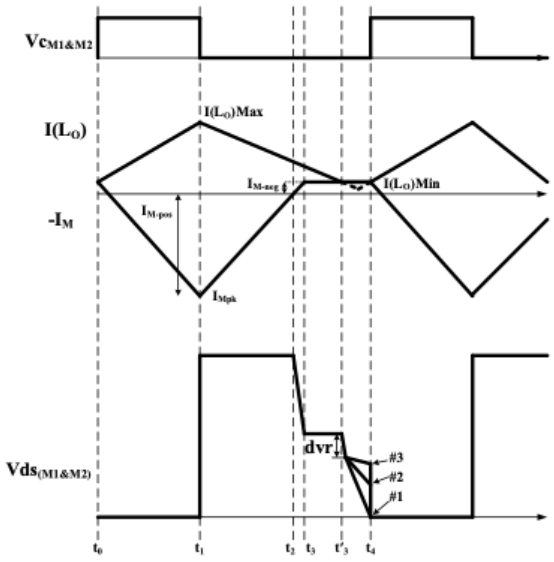

Fig. 6 – Waveforms of the circuit from Fig. 3 [5].

4. ZVS IN FORWARD WITH ACTIVE CLAMP TOPOLOGY BY EMPLOYING THE NEGATIVE MAGNETIZING CURRENT

In Fig. 7 a single ended forward with active clamp topology is presented. This topology was presented in many publications such as references [6–8]. In Fig. 8 the key waveforms from the circuit in Fig. 7 are presented. They depict the control signal for M_1 and M_2, the current through the output inductor L_o, the magnetizing current, the current through M_1, the current through the clamp capacitor C_{CL} and the voltage $V_{ds(M1)}$ across M_1

Interval 1 [t_0 to t_1]: Between t_0 to t_1, the main switch M_1 is on, and the current builds up via the primary winding, L_1, and the main switch M_1 as depicted by $I(M_1)$. During this time, in a forward mode the current is induced in the secondary winding via SR_1, and the output inductor L_o, which is also depicted by the $I(L_o)$. During this time the flux density builds up in the transformer Tr_1, depicted by the $(-I_M)$. At t_1 the main switch M_1 turns off.

Between t_1 and t_1' the voltage builds up across the main switch M_1 via the body diode of M_{CL} and the clamp capacitor C_{CL}.

At t_1' the second switch M_{CL}, referred also as clamp capacitor is turned on. The magnetizing current flows via M_{CL} and C_{CL}. The active clamp is also known as the "current mirror", wherein the magnetizing current looks like is reflected by the C_{CL} capacitor, wherein the magnetizing current amplitude is changing linearly from t_1 to t_3, reaching zero amplitude at t_2 and its peak, $I_{Mpk-neg}$, at t_5.

At t_3 the switch M_{CL} is turned off and the magnetizing current has a negative polarity flowing through parasitic capacitance of M_{CL}, from source to drain, through the primary winding of the transformer Tr_1 and further to the input voltage. The magnetizing current I_M is discharging the parasitic capacitance of M_1 between t_3 and t_4 as depicted by $V_{ds(M1)}$. When the voltage across M_1 decays under V_{in} level, the polarity of the voltage across the secondary winding L_2, changes and the current starts flowing through the body diode of SR_1 and SR_2 which was conducting the current through L_o. The magnetizing current flowing through C_{CL} at t_3 will discharge the parasitic capacitance across M1 between t_3 to t_4 in a resonant way.

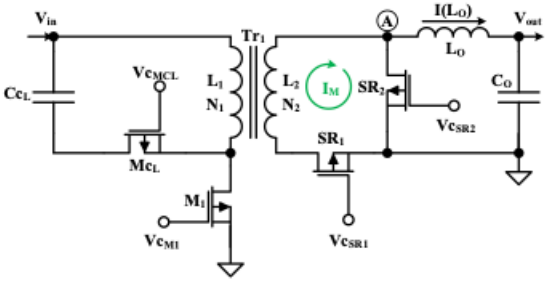

Fig. 7 – Single-ended forward with active clamp [1].

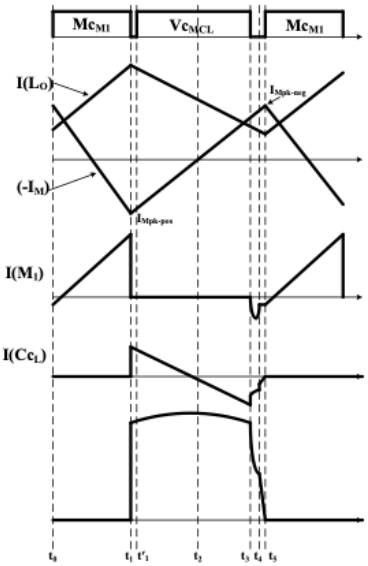

Fig. 8 – Key Waveforms from the circuit presented in Fig. 7.

It is noticeable comparing the $(-I_M)$ from Fig. 4 and the magnetizing current from Fig. 8 which represents the magnetizing current of the single ended forward with active clamp, that the negative magnetizing current amplitude has the same amplitude of the positive magnetizing current and $I_{Mpk-poz}$ is larger than the current through L_o, $I(L_o)$. As a result, the difference between the magnetizing current in between t_4 and t_5 reflects into the primary winding of the transformer Tr_1 and it will discharge the parasitic capacitance across M_1 linearly between t_4 and t_5 towards zero and reach zero at t_5. To obtain ZVS in the circuit presented in Fig.7, the following relation must be satisfied:

$$I_M > \left(I_M - \frac{1}{2} * \frac{V_O(1-D)}{L_O * Freq}\right), \quad (5)$$

where I_M is the magnetizing current reflected in the secondary defined by eq. (2)., V_o is the output voltage. , D is the duty cycle of operation. L_o is the inductance of the output choke and F_{req} is the frequency of operation of the converter.

The ZVS method presented in this paper wherein the ZVS is obtained when the condition from (5) is satisfied works also in other topologies such as half bridge and full bridge. That is

presented in reference [9].

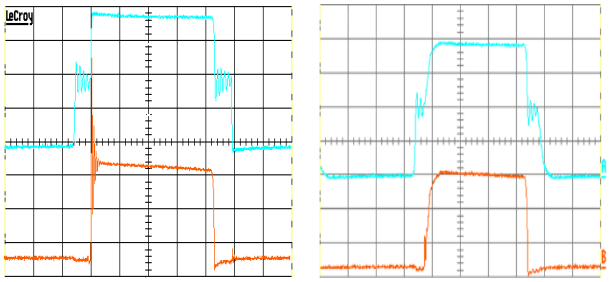

Fig. 9 – Key Waveforms in a half bridge topology in hard switching mode (left picture) and soft switching node (right picture).
Upper trace: Voltage in the switching node in the primary side.
Lower trace: the voltage across the rectifiers in the secondary side.

Figure 9 depicts the voltage in the primary switching node of a half bridge topology and the voltage across the synchronous rectifiers in the secondary taken from the oscilloscope. The left picture depicts these waveforms in hard switching mode and the right picture depicts the waveforms in soft switching mode. The soft switching mode is obtained by using the same method presented in this paper. It is noticeable that using this method for ZVS there are no spikes nor glitches across the secondary synchronous rectifiers, because the secondary synchronized rectifiers turn off at zero current. This solution of obtaining ZVS in applications wherein very low leakage inductance transformers are used, applies also to full bridge topologies as presented in reference [10].

The ZVS method presented in this article ~~is~~ applies also in half bridge and full bridge topology as per reference [3,4,9,10].

This article is the first public disclosure of using this methodology in a single ended forward converter with active clamp. In references [11–13] are presented other methodologies of obtaining ZVS in Forward and full bridge topology in certain operating conditions.

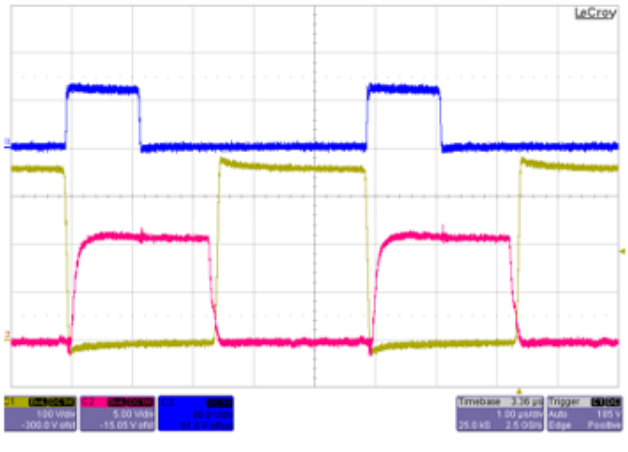

Fig. 10 – Key Waveforms in a phase shifted full bridge topology in soft switching mode using the method presented in this paper.
Blue trace: the voltage across the secondary synchronous rectifiers.
Brown trace: the voltage across the primary switchers.
Red trace: The gate signal on the primary switchers.

In Fig. 10 are depicted the key waveforms, from the oscilloscope, across the secondary synchronized rectifiers, the voltage across the primary switchers and the gate signal in a phase shifted full bridge topology used in a 2 kW, auxiliary battery charger for automotive taken at V_{in} = 345 V, V_o = 12 V, I_o = 90 A. It is noticeable that there are no spikes and glitches across the synchronous rectifiers (blue trace) switching at 90A without the use of snubbers.

In [14] are presented new technologies in planar transformers which decrease significantly the leakage inductance creating coupling coefficient even higher than K > 0.998. Very low leakage inductance obtained in these magnetic technologies is aimed at very high current applications and higher efficiency. In the light of the latest development in magnetic technologies the ZVS method presented in this paper has become a very suitable solution.

The methodology presented in the paper, which combines zero voltage switching in the primary together with zero current switching in the secondary, is the trend in technology which will bring the best performance not only in isolated DC-DC converters but also in inverters [15].

5. CONCLUSIONS

In this paper is presented a methodology of obtaining zero voltage switching for a single ended forward converter using active clamp topology and two transistor forward topology in application wherein the transformer has a very small leakage inductance.

This method is based on having a magnetizing current amplitude larger than the current through the output inductor. The magnetizing current which exceeds the current through the output inductor which occurs prior to the turn on time of the primary switchers, will force the current through the freewheeling rectifier to decrease to zero and the current difference in between the magnetizing current and the current through the output inductor will be pushed back into the primary discharging the parasitic capacitance across the primary switchers to zero. This method of ZVS operates independent of the leakage inductance and creates zero voltage switching in all the operating conditions once the inequality (5) is satisfied and creates zero current switching through the freewheeling rectifier. Using this methodology there are no spikes or glitches and there is no need for snubbers across the freewheeling rectifier.

REFERENCES

(1) I. Jitaru, *High efficiency DC–DC converter*, International Power Conversion & Intelligent Motion, PCIM '94, Twenty-Eight International, pp. 880–887 (1994).

(2) I. Jitaru, *Constant frequency, forward converter with resonant transition*, High Frequency Power Conversion, HFPC '91, Sixth International, Ventura, Calif. (1991).

(3) I. Jitaru, *Soft transition on all switching elements two transistors forward converter*, US-9,899,929-B2 (2018).

(4) I. Jitaru, *True soft switching by timed steering of a current source*, US-10,050,545-B2 (2018).

(5) I. Jitaru, *True ZVS solutions in forward topologies*, 63/757740 (2025).

(6) I. Jitaru, *A new high frequency, zero-voltage switched, PWM converter*, [Proceedings] APEC '92 Seventh Annual Applied Power Electronics Conference and Exposition, Boston, MA, USA, pp. 657–664 (1992).

(7) I. Jitaru, *Constant frequency zero voltage PWM converters*, International Power Conversion & Intelligent Motion, PCIM '92, Twenty-Fourth International (1992).

(8) I. Jitaru, *High frequency, soft transitions converter*, Proceedings Eighth Annual Applied Power Electronics Conference and Exposition, San Diego, CA, USA, pp. 880–887 (1993).

(9) I. Jitaru, *Soft switching converter by steering the magnetizing current*, US-10,103,639-B2 (2018).

(10) I. Jitaru, *Phase-shifted full-bridge topology with current injection*, US-10,291,140-B2 (2019).

(11) J. Xu, X. Cao, Q. Luo, *An improved two-transistor forward converter*, Proceedings of the IEEE 1999 International Conference on Power Electronics and Drive Systems. PEDS'99, pp. 225–228 (1999).

(12) N.H. Kutkut, D.M. Divan, R.W. Gascoigne, *An improved full*

bridge zero-voltage switching PWM DC-DC converter using a two inductor rectifier, Conference Record of the 1993 IEEE Industry Applications Conference Twenty-Eighth IAS Annual Meeting, pp. 1065–1072 (1993).

(13) T.A. Pereira, et al., *Optimal design of planar transformer for GaN based phase-shifted full bridge converter*, 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 2241–2248 (2020).

(14) I. Jitaru, *Magnetic structure for low leakage inductance and very high efficiency*, US-10,937,590 (2021).

(15) A. Chakrabarti, P. Kumar Sadhu, P. Pal, *A novel dead-time elimination strategy for voltage source inverters in induction heating systems through fractional order controllers*, Rev. Roum. Sci. Techn. – Électrotechn. Et Énerg., **67**, *2*, pp. 181–185 (2022).