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FAULT-TOLERANT, CAPABLE, AND SCALABLE TWO-TIME-SCALE BOOST CONVERTER MEANT FOR RESIDENTIAL AREAS

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The feasibility of next-generation urban power networks hinges on the ability of DC converters to replace their conventional counterpart. Reliability and efficiency are heavily contested points when discussing the challenges facing power electronics proliferation in power systems. Motivated to find a working solution, this paper presents the paradigm of the two-time scale converter. By employing a division in dynamics, interpreted from singular perturbation theory, a cost-effective redundancy can be attained in the form of complementary fast and slow subsystems. This enables the proposed converter to handle considerable perturbations with a quick response time and achieve cost-effective operation at steady state, thanks to the reduction in switching frequency. The overall controller scheme comprises an inner current control loop and an outer voltage control loop; the control laws are derived from a generic Lyapunov approach, which can be adapted to the characteristics of the voltage source. The simulation results demonstrated a seamless response to various types of perturbations and the proper handling of different omission fault scenarios.

1. INTRODUCTION

In recent years, in both the private and industrial sectors, a noticeable rise in DC load consumption catapulted DC power systems into a position of prominence [1]. The supply of DC power finds market applications in various sectors, including electric vehicles, Electric Storage Systems (ESS), laptops, smartphones, and LED lighting. That being the case, a modern power system should accommodate legacy AC equipment; as such, the implication of connecting the DC bus to an inverter should be thoroughly investigated [2,3]. Another article of interest to the endeavor is the use of power converters in the MG. The choice of topology plays a critical role in determining the quality of power flow control. Some of these may perform the same task with varying differences in characteristics, entailing an in-depth study of different aspects such as efficiency, cost, robustness, isolation, power density, and power rating [4,5].

When supplying energy to sensitive loads or critical infrastructure, end-users expect both high-quality and reliable service. This includes a robust response to sudden, unpredictable changes in the power system, whether it is a slight disturbance such as the sudden connection or disconnection of loads or significant disturbances (*e.g.*, the disconnection of a source or a change in system parameters), implying different arithmetic methods respective of their dynamics [6]. Constructing an MG that caters to such loads is a multi-criteria problem, which includes. Still, it is not limited to the cost and capacity of installation, power electronics performance, and fault-tolerant capabilities.

In [7], a study was conducted on the senseless nonlinear control of packed U-cell converters, employing a Lyapunov approach to ensure asymptotic stability in the context of a grid-connected photovoltaic (PV) system. Another Lyapunov approach-based study in [8] focused on power density and efficiency, implementing a fast and stable sliding mode controller for a DC-DC boost converter. The study addressed nuances such as chattering phenomena, perturbation mitigation, and the tradeoff between cost-effectiveness and performance. The work in [9] proposes a novel high-gain DC-DC converter, with a focus on maximum power point tracking applications. By employing a voltage-doubling-based topology, the converter achieves high efficiency while also ensuring both efficiency and longevity. The work in [10] presents a novel approach to emulating a proton exchange membrane fuel cell using a DC-DC buck converter. The constructed emulator converter finds its application in reducing current ripples and alleviating stress on power switches. Additionally, the published work utilizes a linear quadratic regulator to control the output voltage of an interleaved boost converter, which reportedly enables a wide range of operation under various loading conditions.

This paper proposes a subtle modification to the classic two-phase boost converter, alongside a control strategy developed to counter different types of perturbations that occur at the DC output. This is done by utilizing Lyapunov's criterion of stability in conjunction with the analogy of singular perturbation-based theory [11]. A hybrid fast-slow type controller is implemented at the outer loop to regulate the output voltage. The ensemble, comprising the "proposed fault-tolerant converter" and the "fast-slow control strategy", enables fault ride-through to occur spontaneously without relying on fault detection.

The content of this paper will be organized as follows: in section 2, the classic boost converter is presented; its model, schematics, and design process of its controller will serve as a reference point and a template for the subsequent analysis. Section 3 discloses the schematics, mathematical formulation, and simulation of the proposed design. In section 4, a case study of different fault types is conducted, followed by a demonstration of multisource integration and scalability. Finally, in section 5, a conclusion is presented that compiles all the obtained results, discussions, and observations into a summarizing script.

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2. CLASSICAL BOOST CONVERTER

A boost converter is a simple yet surprisingly versatile converter, it is used in different applications. Consider the model (1) of a simple boost converter [12], in Fig. 1.

$$\begin{bmatrix} \frac{di}{dt} \\ \frac{dV_{out}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{(1-u)}{L} \\ \frac{(1-u)}{C} & -\frac{1}{CR_{Load}} \end{bmatrix} \begin{bmatrix} i \\ V_{out} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} E, \quad (1)$$

Where the control gate signal "u" represents the conduction state of the power switch — ON for "u=1" and OFF for "u=0" — "i" is the input current, E and V_{out} are the input and output voltages respectively, C, L and R_{Load} are the converter's output capacitance, input inductance and output load respectively.

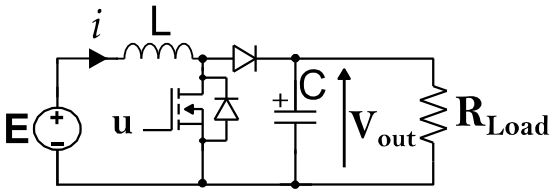

Fig. 1 – Schematic of a boost converter.

To drive this converter, a dual loop control scheme is adopted, consisting of two loops, an outer loop for voltage and an inner loop for current, as described in Fig. 2.

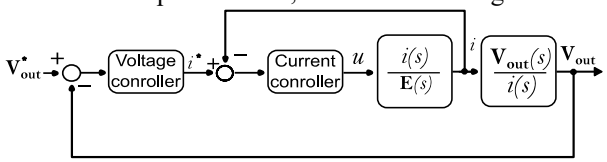

Fig. 2 – Block diagram of a regulated boost converter.

Consequently, the control problem is broken down into two interrelating subsystems, one is described in eq. (2) which relates the input voltage to the input current and another in eq. (3) which relates the input current to the output voltage.

$$\frac{i(s)}{E(s)} = \frac{\left(s + \frac{1}{CR_{Load}}\right)}{L\left(s\left(s + \frac{1}{CR_{Load}}\right) + \frac{(1-u)^2}{LC}\right)}, \quad (2)$$

$$\frac{V_{out}(s)}{i(s)} = \frac{(1-u)}{C\left(s + \frac{1}{CR_{Load}}\right)} \quad (3)$$

For eq. (3), it is easily obtained by applying the definition of State-Space to Transfer Function conversion, similarly eq. (2) is obtained by applying the definition and additionally substituting eq. (3) for V_{out}.

2.1 CURRENT CONTROL

The current control of the converter can be implemented by employing a generic Lyapunov's stability approach in the form of a sliding mode controller (SMC), starting from the differential equation of the current which is derived from the state space representation in eq. (1)

$$\frac{di}{dt} = \frac{E}{L} - \frac{(1-u)}{L} V_{out}, \quad (4)$$

By applying the definition of the sliding surface [14] in equation (5) for n=1 and $\tilde{x} = i - i_d$, i_d being the desired current reference and "i" the real measured current, a sliding surface denoted S is recognized in

$$S(x;t) = \left(\frac{d}{dt} + \lambda\right)^{n-1} \tilde{x} = \left(\frac{d}{dt} + \lambda\right)^{0} (i - i_d), \quad (5)$$

where x is the controlled state and λ is a positive linear coefficient. The surface derivative is denoted in equation (6) [12].

$$\dot{S} = \frac{E}{L} - (1-u)\frac{V_{out}(t)}{L}, \quad (6)$$

Through choosing a generic candidate function denoted B

$$B = \frac{1}{2}S^2 \text{ and } \dot{B} = S\dot{S}, \quad (7)$$

The condition of stability can be analyzed in

$$\dot{B} = \dot{S}S = \left(\frac{E}{L} - (1-u)\frac{V_{out}(t)}{L}\right) S < 0, \quad (8)$$

The gate driving signal u is a discrete variable of values 0 or 1 and it is dependent on the surface S, a control law is adopted from [15],

$$u = \frac{1 - \mathrm{sgn}(S)}{2}, \quad (9)$$

Checking the validity of the control law by applying the criterion and for a negative surface (*i.e.*, $i_d > i$),

$$\left(\dot{S}S = -|S|\frac{E}{L}\right) < 0. \quad (10)$$

since the voltage source E is considered a positive non null value the criterion is fulfilled for $\mathrm{sgn}(S) = -1$. The same analogy is applied to the positive value of the surface

$$\left(\dot{S}S = |S|\frac{E - V_{out}(t)}{L}\right) < 0. \quad (11)$$

To Show case the validity of the current control a simulation is ran is Fig. 3, with an initial current of 0 A and a desired reference of 10 A.

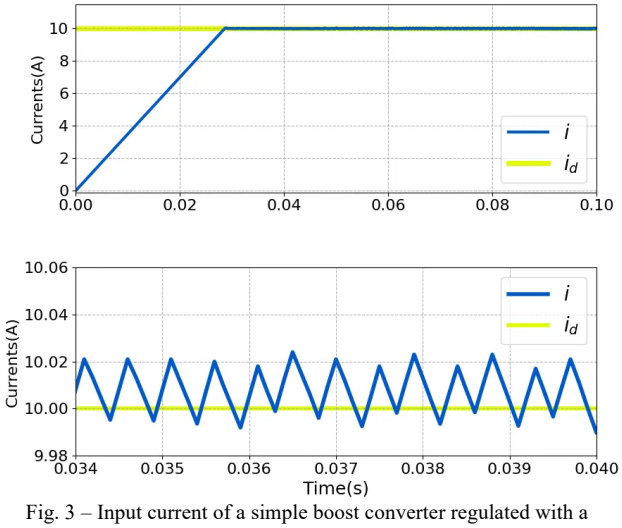

Fig. 3 – Input current of a simple boost converter regulated with a SMC: (top plot) over all profile over 100ms; (bottom plot) a close up to the reference point from 34ms to 40ms.

The current control is stable as long as $V_{out} > E$, the following expression denotes the stability condition for a positive surface. The reach time t_{reach} can be expressed as

$$\begin{cases} \text{For } S < 0;\ t_{reach} = \dfrac{|S(t=0)|L}{E}, \\ \text{For } S > 0;\ t_{reach} = \dfrac{|S(t=0)|L}{|E - V_{out}(t)|}. \end{cases} \quad (12)$$

Following its sliding mode controller which is derived from its law in eq. (9). A close on the graph in Fig. 3 (bottom) reveals the shattering of the SMC, the frequency at which this controller operates, and the inductors value dictate the severity of the shattering.

2.1 VOLTAGE CONTROL

A PI controller can be deployed for voltage regulation at the outer loop. In the simulation, the Input voltage is set to 30V, the reference voltage to 50 V and the initial voltage of the capacitor is set to 30V. The impact of a sudden step perturbation on this control is observed in Fig. 4 at time t=7.5s, with a jump in load from 2A to 4A.

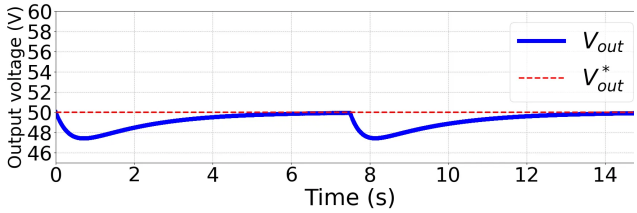

Fig. 4 – Step perturbation of the output voltage of a PI controlled boost converter.

Steady state is achieved afterward at time t=10s, A voltage drop of 3V is observed and the recovery time is approximately 3s. In order to ensure adequate performance, the inner current loop must exhibit fast response time in order to overturn the perturbation.

$$\frac{di}{dt} \gg \frac{di_d}{dt}. \quad (13)$$

3. TWO-TIME SCALE BOOST CONVERTER

In this section, the concept of the Two-Time Scale (TTS) converter is presented. Consider a two-phase boost converter in Fig. 5, consisting of two arms where inductors L1 and L2 are of different values.

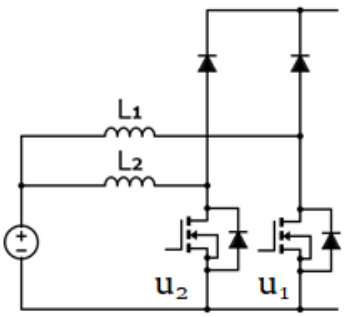

Fig. 5 – schematic of a two-time scale converter.

The converter's currents differential equations are

$$\begin{cases} \dfrac{di_1}{dt} = \dfrac{E}{L_1} - \dfrac{(1-u_1)}{L_1} V_{out} \\ \dfrac{di_2}{dt} = \dfrac{E}{L_2} - \dfrac{(1-u_2)}{L_2} V_{out} \end{cases}, \quad (14)$$

where u_1 and u_2 are the gate conduction states, whereas i_1 and i_2 are the input currents. A fast-slow system, also called Two-Time Scale systems [16], is a type of systems is characterized with having a two horizontally separable clusters of poles in Laplace domain. equation (15) describes such systems as

$$\begin{cases} \dot{X} = A_{11}X + A_{12}Z + B_1U \\ \varepsilon\dot{Z} = A_{21}X + A_{22}Z + B_2U \end{cases}, \quad (15)$$

where X is the slow state vector, Z is the fast state vector, U is the control input, ε is a small positive parameter highlighting the time-scale separation between system dynamics, and A_{11}, A_{12}, A_{21}, A_{22}, $B_1$and B_2 are constant matrices of appropriate dimensions that define the system dynamics. The inductors are chosen such that they are related by a "small" parameter ε,

$$\varepsilon L_1 = L_2, \quad (16)$$

A naturally decoupled system, eq. (17), is produced when matrix A_{12} and A_{21} in eq. (15) are null

$$\begin{cases} \dot{X}_s = A_s X_s + B_s U_s \\ \dot{X}_f = A_f X_f + B_f U_f \end{cases} \quad (17)$$

Where the subscript "s" and "f" refer to the terms slow and fast respectively. For a sufficiently small ε relating L_1 to L_2 the separation of dynamics between the system's states is justified, hence eq. (14) is redefined,

$$\begin{cases} \dfrac{di_s}{dt} = \dfrac{E}{L_1} - \dfrac{(1-u_s)}{L_1} V_{out} \\ \dfrac{di_f}{dt} = \dfrac{E}{L_2} - \dfrac{(1-u_f)}{L_2} V_{out} \end{cases} \quad (18)$$

i_1 becoming the slow current i_s, i_2 the fast current i_f u_1 the slow gate control u_s and u_2 the fast gate control u_f.

3.1 TTS CURRENT CONTROL

A state feedback control law for this sort of systems [11]

$$U = U_f + U_s, \quad (19)$$

where U, U_f and U_s are total, fast and slow controllers output. to ensure that the fast control converges to zero in steady state, its surface is defined such that its desired value diminish in proportion to the slow current,

$$\begin{cases} S_s = i_1 - i_d \\ S_f = i_2 - i_{df} \end{cases} \text{ and } i_{df} = (i_d - i_1), \quad (20)$$

where i_{df} is the desired fast current, the control signal u_f and u_s are derived from

$$\begin{cases} u_s = \dfrac{1 - \text{sgn}(S_s)}{2} \\ u_f = \dfrac{1 - \text{sgn}(S_f)}{2} \end{cases}, \quad (21)$$

The stability analysis of the slow surface carries out the same in eqs. (4) through (11), similarly for the fast surface, we substitute the definition of the desired current in the fast surface and repeat the same procedure.

$$\dot{S}_f S_f = \left(\begin{array}{c} \left(\frac{E}{L_{eq}}\right) - (1-u_f)\left(\frac{V_{out}(t)}{L_2}\right) \\ -(1-u_s)\left(\frac{V_{out}(t)}{L_1}\right) \end{array} \right) S_f < 0 \quad (22)$$

In eq. (22), *i.e.*, the stability analysis of the fast subsystem, an additional stability criterion can be deduced and highlighted in Table 1.

Table 1

Stability analysis of the TTS converter.

	$u_s = 1$
$u_f = 1$	$\dot{S}_f S_f = -\left(\frac{E}{L_{eq}}\right) \lvert S_f \rvert < 0$
$u_f = 0$	$\dot{S}_f S_f = \left(\frac{E}{L_{eq}} - \frac{V_{out}(t)}{L_2}\right) \lvert S_f \rvert < 0$

	$u_s = 0$
$u_f = 1$	$\dot{S}_f S_f = -\left(\frac{E}{L_{eq}} - \frac{V_{out}(t)}{L_1}\right) \lvert S_f \rvert < 0$
$u_f = 0$	$\dot{S}_f S_f = \left(\frac{E}{L_{eq}} - \frac{V_{out}(t)}{L_2} - \frac{V_{out}(t)}{L_1}\right) \lvert S_f \rvert < 0$

The small parameter ε must be adequately small enough in value for this control to be stable, the condition of stability is thus denoted

$$L_1 \gg L_2, \quad (23)$$

with

$$L_{eq} = \frac{L_1 L_2}{L_1 + L_2} \approx L_2. \quad (24)$$

To demonstrate the validity of the devised current control a simulation is ran in Fig. 6. The TTS converter's input current is derived to constant reference of 1 A. The current of the Fast Arm (FA) "i_f" (Fig. 6 top graph) reaches the desired value much faster than the Slow Arm's (SA) current "i_s" (Fig. 6 middle graph), then decay to zero in proportion, as the SA approaches the desired value. Their combined value "I_{total}" (Fig. 6 bottom graph) assures fast response time in transient and minimum switching losses in steady state since the slow arm can operate at lower switching frequencies.

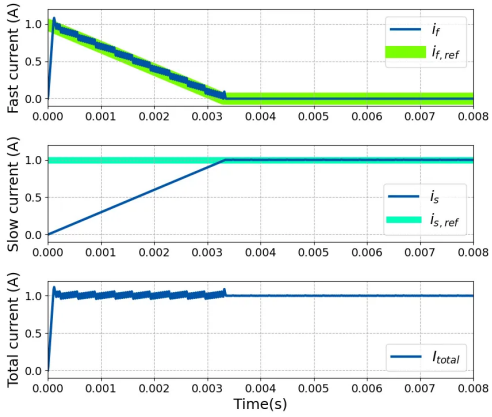

Fig. 6 – Fast and Slow currents of the TTS boost.

3.2 TTS VOLTAGE CONTROL

A two-time scale boost converter assures fast response to perturbation with optimal efficiency; this is attained by aggregating the dynamics of two complimentary subsystems.

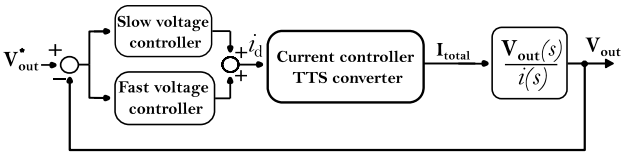

Fig. 7 – Voltage control schematics of the TTS converter.

The controllers designed for this simulation regulate the voltage at 45 V. A tolerance zone is established between 45.5 V and 44.5 V respectively. The slow controller is a "weak" PI controller with bounded input and output. The fast control is a high gain state feedback controller that reacts only when the tolerance is crossed. In order to display the performance of the TTS converter, it is submitted to incremented perturbation. In Fig. 8, the converter is subjecting to a step perturbation that causes the output voltage to deviate from the tolerance zone. Then, the fast controller is prompted to respond, hurling the voltage back to the tolerance region.

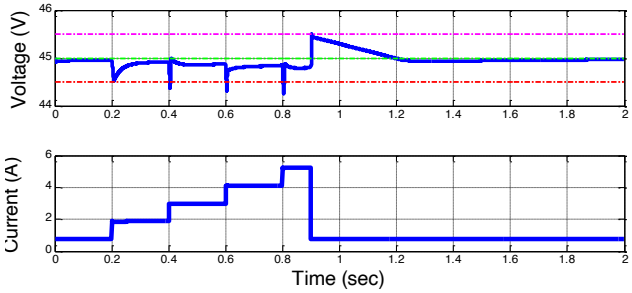

Fig. 8 – Slow and fast current (Step load)

Conversely, when a load is abruptly disconnected, a pull-down mechanism is triggered temporarily. This can be realized via a battery system, however, due to the random or periodic nature of these perturbances, and considering that an ESS limits its charging and discharging cycles, with the intended interest of extend its lifespan [17], a super capacitor may be connected instead through a synchronous boost converter, allowing for the surplus energy to find a path to be stored or dissipated. In Fig. 10, a sudden jump in current happens every 0.2 s starting from t = 0 s until 0.8 s, at t = 0.9 s a sudden disconnect of the load occurs prompting the overvoltage mechanism to handle the surplus energy.

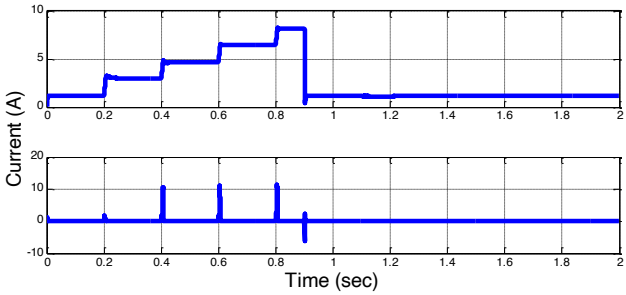

Fig. 9 – Slow current (top plot) and fast current (bottom plot) input current.

3.3 BI-DIRECTIONAL CONVERTER

The synchronous boost converter in Fig. 10, can handle a bi-directional flow of current both to supply and store energy. When charging, the power is "sourced" from the output voltage V_{out} bus, into the input terminals of the battery.

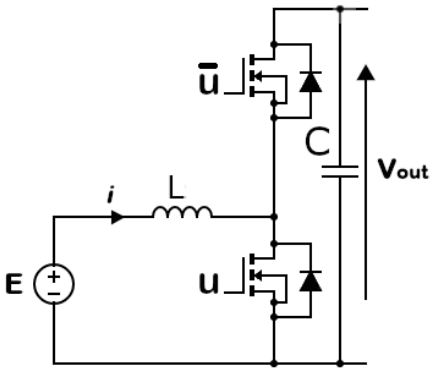

Fig. 10 – Schematic of a synchronous boost converter.

Conversely, when discharging, the power flows in the opposite direction,

$$V_L = V_{(reg)} - V_{(source)}, \tag{25}$$

where V_L is the inductance's voltage, $V_{(reg)}$ the regulated voltage and $V_{(source)}$ the source voltage. The operation mode coefficient "m" used in, refers to the operation mode, when discharging the converter is set in boost mode and m = 1, when charging the converter is set in buck mode and m = 0.

$$\begin{cases} V_{(reg)} = m\delta V_{out(reg)} + (1-m)E_{(reg)} \\ V_{(source)} = (1-m)(1-\delta)V_{out(source)} + mE_{(source)} \end{cases} \tag{26}$$

where δ is the duty cycle of the gate signal [18]. Applying the concepts discussed in previous subsections, a bi-directional two-time scale converter, as illustrated in Fig. 11, is achieved.

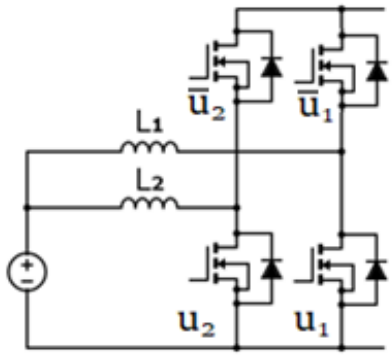

Fig. 11 – Schematic of a synchronous TTS synchronous boost converter.

The control law in eq. (21) works for both positive and negative values of the desired reference. The synchronous converter reference is set to -1 A current at t = 0.5 s Fig. 12 (most bottom graph).

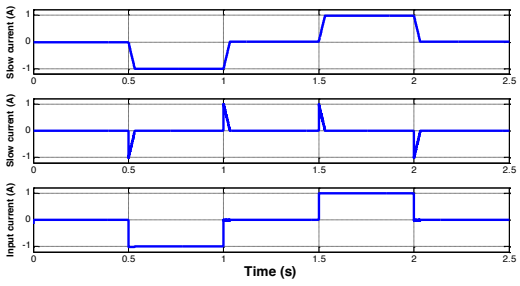

Fig. 12 – Current profile of the synchronous two-time scale converter.

At the transients, the FA supplies a fast surge of energy at, then the power decays to zero, as the slow current raises. At t = 1 s the current reference is set to zero and it is observed that the fast current counter the direction of the slow one achieving a net zero current at the output current. Conversely, at time t = 1.5 s the reference is set to 1 A. the FA of the converter assists with transition, providing a burst of energy that propels the net current to the desired value, then gradually decays as the SA pick up the load.

4. FAULT TOLERANCE

This paper focuses on omission faults (open circuit). To visualize the effect of disconnecting different subsystems, a simulation was conducted according to chronological fault order in Fig. 13. A value of 1 represent an ON or enabled state whereas a value of 0 indicate an OFF state or disabled. After disabling a component, the system is subjected to a step perturbation of 5 A that lasts 0.2 s, then the test component is restored into the enabled state while another is disabled as preparation for the next perturbation test.

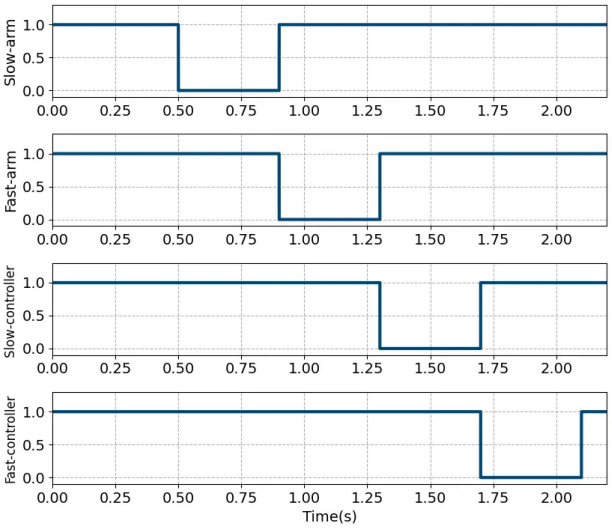

Fig. 13 – Fault timing.

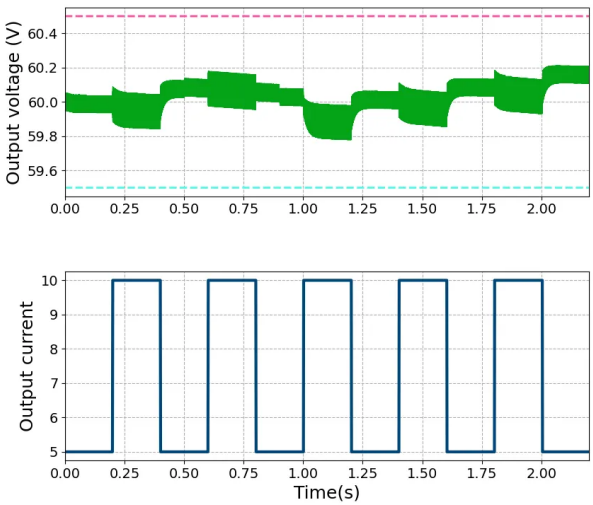

Fig. 14 – Fault simulation results.

At time t = 0 in Fig. 14 (bottom plot), the converter outputs a constant current of 5 A, this continues until t = 0.2 s where a step perturbation of an additional 5 A is added to the load, this is done to highlight normal behavior of the converter.

The first incurred fault is the loss of the SA; this is the most likely scenario as the FA works mostly in standby mode. At time $t = 0.5$ s the SA is disconnected then a step perturbation of an additional 5 Amps is engaged at $t = 0.6$ s. The observed output voltage Fig. 14 (upper plot), of the converter remains within the tolerance zone.

It is noteworthy that in fault ride-through mode, where the SA is disabled, the FA is subjected to significant stress when operating for a prolonged period, hence degradation occurs at accelerated rates. At time $t = 0.9$ s, the SA is back online, and the FA is disconnected, then at $t = 1$ s, the system is subjected to the same previous perturbation. This time, a noticeable voltage dip can be observed in the output voltage falling below the minimum tolerance level; the system, however, regains stability and continues its operation. Since the converter relies on the FA for the fast response, it is only natural that such underperformance would occur. Next, at $t = 1.3$ s, both arms are enabled instead of the PI controller, which is disconnected. Again, the converter continues to function normally. Lastly, at $t = 1.7$ s, the PI controller is reactivated, and the fast controller is disabled; this time, the system continues to hold the voltage at the limit of its tolerance.

5. CONCLUSIONS

In this paper, a TTS converter has been designed and simulated, yielding promising results, particularly in terms of robustness. The fast and slow arms assure both optimal efficiency and adequate performance. Due to the redundancy in the system, the converter is fault-tolerant; furthermore, it offers additional degrees of freedom regarding power management and power scalability. The synchronous version of the two-time scale converter can achieve greater efficiency and, more importantly, bi-directional flow of electrical energy, hence it can be implemented in ESS. Surplus energy that would lead to an overvoltage at either side of the converter is absorbed via a super capacitor in conjunction with thermal dissipation. Various techniques can be implemented to achieve voltage regulation; the selection of the proper strategy considers the level of robustness required.

AUTHOR CONTRIBUTIONS

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All authors have read and agreed to the published version of the manuscript.

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