ANALYSIS AND EXPERIMENTAL VALIDATION OF A NON-ISOLATED DC-DC SEPIC-MODIFIED CUK COMBINED CONVERTER

MURALI DURAISAMY

Keywords: Experimental setup; Integrated non-isolated DC-DC power converter; MATLAB/Simulink model; Nonzero inductor current; Semiconductor components' voltage stress; Static voltage gain; Steady state operating modes.

The power can be generated using non-conventional energy sources. However, these sources are intermittent and unpredictable. Thus, the consumer power supply is not continuous. However, the combination of two or more non-conventional resources can make the supply continuous. The research proposal presented in this work explores an integrated non-isolated DC-DC power converter structure that has the parallel combination of traditional SEPIC (single-ended primary inductor converter) and voltage-gain-boosted Cuk configurations. The features of the proposed DC-DC power conversion structure include nonzero current flow through inductors, a reduced number of inductors and capacitors in the topology, reduced voltage stress on semiconductor-based components, and a relatively high step-up voltage gain. The operating modes of the topology are explored along with the derivation of the static voltage gain. To validate the effectiveness of the proposed integrated converter structure, an experimental setup is developed, and its results are compared with those of the MATLAB/Simulink model of the topology.

1. INTRODUCTION

The global demand for electrical energy is increasing steadily. To meet the increasing energy demand for industrial and commercial consumers, both conventional and nonconventional energy sources are employed. The efficiency of power generation using conventional fossil fuels, such as coal, oil, and natural gas, is high. However, coal burning causes environmental pollution globally and a sudden increase in surface temperature on the Earth. Furthermore, conventional sources of energy are non-renewable, with limited availability. Once these resources deplete, their formation may take millions of years [1]. Non-conventional methods, such as solar, wind, and biomass energy, are another choice for power generation [2,3]. Solar energy produces low-level DC voltages, typically ranging from 20 V to 40 V only [4]. This low-level DC input voltage cannot drive the gridconnected inverters. Hence, a power electronic interface, such as a DC-DC converter, is required for converting the lowlevel DC voltage produced by solar panels into a high-level DC voltage suitable for driving the inverters. There are nonisolated and isolated structures of DC-DC converters discussed in the literature [5-15]. Each configuration has its own features and limitations [16]. The suitable choice of topology is based on the applications [17–19].

A non-isolated, modified single-switch, highly efficient SEPIC structure is presented in [20], which shows a relatively improved static gain based on magnetic coupling and low voltage stress across the power switch. Another modified structure of a single-switch configured SEPIC topology with enhanced voltage gain is proposed by some authors in [21], where the hardware results are given to validate the converter's performance. A high-reliability traditional SEPIC topology with extended units can be designed to feature a reconfigurable voltage gain with a wide range [22]. A single-switch configured high-gain SEPIC topology is presented in [23], suitable for DC microgrids.

A transformer-less modified Cuk topology with required voltage multiplier cells is suggested by some authors [24]. The configuration proposed in [24] can achieve a relatively high voltage conversion ratio at a low duty ratio of the power switch. A Cuk-based DC-DC converter is suggested in [25], in which the voltage-lift technique is employed to achieve both high converter efficiency and improved voltage gain. A smaller-sized coupling capacitor with a low voltage rating can

produce relatively improved power converter efficiency in a conventional Cuk configuration, resulting in reduced size [26].

A non-isolated boost-Cuk combined DC-DC converter structure can produce enhanced static voltage gain [27]. The steady-state operating modes and time domain modeling of the hybrid converter are explored in [27]. Specific nonisolated configurations of DC-DC converters derived from the boost topology are reviewed in [28], which are suitable for smart grid applications. The steady-state performance comparison of all high-gain topologies is explored in [28], where theoretical and simulation results are also provided to validate the performance. Some authors proposed an isolated category of hybrid two-stage DC-DC converter structure suitable for high-power HVDC applications [29]. The features of the converter proposed in [29] include superior performance over a wide input voltage range and suitability for high-power applications. Theoretical analysis, component design, and experimental setup are also provided for performance validation [29].

The DC-DC power electronic conversion topologies with reduced component count, which can achieve enhanced voltage gain, improved converter efficiency, and low switch voltage stress, are proposed by some authors [30,31]. A magnetically integrated structure of the conventional boost and Cuk configurations is proposed in [32] to achieve an improved voltage conversion ratio and high-power density using a switching inductor. The converter suggested in [32] features a single power switch and exhibits lower ripple levels in both source and load currents, which are continuous. A single-switch, hybrid DC-DC converter with dual outputs, combining the Cuk and SEPIC topologies, is suggested by some authors [33] for solar PV applications. This configuration utilizes an integrated magnetic core to reduce ripples in the input current and achieve improved power extraction from the solar PV system. The simulation and hardware implementation of the converter suggested in [33] demonstrates its effectiveness. Some authors have suggested a new integrated configuration of conventional boost, Cuk, and forward converters for high-voltage gain applications [34]. The structure proposed in [34] exhibits the characteristics of an input current with no ripples and reduced switch voltage stress, achieved through the use of two inductors. The converter topology suggested in [34] is operated in discontinuous conduction mode and is demonstrated with hardware results for the effectiveness of

¹ Government College of Engineering Srirangam, Tiruchirappalli, India. E-mail: muralid@gces.edu.in

its performance.

The projected work in this paper explores steady-state operating modes using equivalent circuits. It provides a practical illustration of a non-isolated hybridized DC-DC converter structure that combines the conventional SEPIC and Cuk topologies with a voltage boosting module. The features of the suggested hybrid converter show relatively improved static voltage gain and reduced voltage stress across the power semiconductor switches. The proposed converter operates in continuous inductor current mode, and therefore, the source current remains constant.

The various portions of the entire research proposal include (i). The steady state operating modes with relevant equations and equivalent circuits of the proposed converter, (ii). The converter simulation analysis was carried out in the MATLAB/Simulink platform (iii). Experimental validation of the converter along with the comparison of results of simulation and hardware model, and (iv). The highlights of the converter are summarized in the conclusion section.

2. THE PROPOSED NON-ISOLATED DC-DC SEPIC-MODIFIED CUK COMBINED CONVERTER

This section examines the behavior of the proposed converter during steady-state operation. The steady state operating modes are explained in detail, along with the converter equivalent structures and relevant equations. The flux balance relationship of the continuous current-carrying inductors is employed to derive the static voltage gain (G) of the converter in terms of duty ratio (δ) .

Figure 1 illustrates the power circuit configuration of the proposed non-isolated DC-DC power electronic conversion topology, which integrates the traditional SEPIC and Cuk topologies with a voltage boosting module. The traditional SEPIC and Cuk topologies are energized separately by two input DC sources Vin. The proposed configuration utilizes ideal components, including two power MOSFET switches (S1 & S2), four diodes (D1-D4), four inductors (L1, L2, L3, and L0), four capacitors (C₁, C₂, C₃, & C₀), and a load resistor (R₀). In this work, the traditional SEPIC and Cuk topologies, along with a voltage boosting module, are integrated in a way that the resultant converter topology ensures an enhanced voltage conversion ratio at a low switch duty factor. Furthermore, semiconductor-based components experience relatively low potential stress. The different operating modes of the converter are illustrated in the following paragraphs.

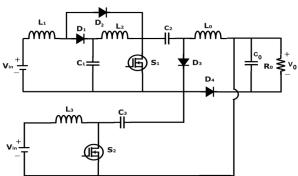


Fig. 1 – Suggested non-isolated hybrid DC-DC power converter topology.

The Mode-I operation of the converter is shown in Fig. 2. The pulse-width-modulated (PWM) signals are supplied to the two switches S_1 & S_2 , to turn them on. The diodes D_1 , D_3 , and D_4 do not conduct because reverse bias voltages

appear across them. The diode D_2 only conducts. The inductors L_1 and L_3 are charged from the source V_{in} through D_2 , S_1 , and S_2 . The inductors L_2 and L_0 are charged due to the discharge of capacitors C_1 , C_2 , and C_3 , respectively. The voltage levels of the inductors are given below (Eq. 1):

$$V_{L1} = V_{in};$$
 $V_{L2} = V_{C1};$ $V_{L3} = V_{in};$ $V_{L0} = V_{C2} + V_{C3}.$ (1)

Fig. 2 – Mode-I operation of the converter.

Figure 3 illustrates the Mode-II operation of the converter. The switch S_1 remains in the conducting mode, while switch S_2 is not conducting. The diodes D_2 and D_4 are conducting, but the diodes D_1 and D_3 are not allowed to conduct. The inductor L_2 gets charged by the discharge of capacitor C_1 . The voltage levels of the inductors are given as Eq. 2 below:

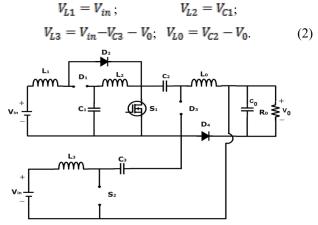


Fig. 3 – Mode-II operation of the converter.

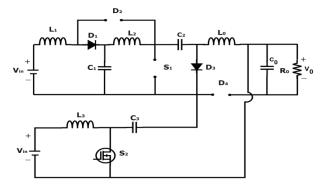


Fig. 4 – Mode-III operation of the converter.

Figure 4 shows the configuration of the proposed converter during Mode-III. Here, the conducting devices are S₂, D₁, and D₃, respectively. The devices that are not conducting are respectively S₁, D₂, and D₄. The charging of

the inductor L_0 is accomplished by discharging the capacitor C_3 . Similarly, the inductor L_2 is magnetized through the discharge of the capacitor C_2 . The voltage levels of the inductors are given as Eq. 3 below:

$$V_{L1} = V_{in} - V_{C1}$$
; $V_{L2} = V_{C1} - V_{C2}$; $V_{L3} = V_{in}$; $V_{L0} = V_{C3}$.(3)

The Mode-IV operation of the topology is explained in Fig. 5. Here, the non-conducting devices are S_1 , S_2 , and D_2 , respectively. The conducting devices are respectively D_1 , D_3 , and D_4 . The capacitor C_1 is charged through the discharge of the inductor L_1 . Similarly, capacitor C_2 gets charged by the discharge of inductor L_2 through the path containing diode D_3 . The capacitor C_0 is charged by the discharge of the inductor L_0 , which in turn charges the capacitor C_0 . The voltage levels of the inductors are:

$$V_{L1} = V_{in} - V_{C1};$$
 $V_{L2} = V_{C1} - V_{C2}$
 $V_{L3} = V_{in} - V_{C3} - V_{0};$ $V_{L0} = -V_{0}.$ (4)

The static voltage conversion ratio (M) in open loop mode of the proposed hybrid converter is derived using the above inductor eq. (1) to (4). The flux balance principle is applied to all the inductors for the purpose of obtaining the following eq. (5) to 10 to derive eq. (11).

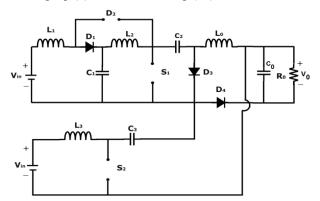


Fig. 5 – Mode IV operation of the converter.

$$V_{in}\delta T_s + (1 - \delta)(V_{in} - V_{C1})T_s = 0.$$
 (5)

Equation 6 gives the following capacitor voltages:

$$V_{C1} = \frac{V_{in}}{(1-\delta)}; V_{C2} = \frac{V_{in}}{(1-\delta)^2}$$
 (6)

$$V_{C1}\delta T_s - (1 - \delta)(V_{C1} - V_{C2})T_s = 0.$$
 (7)

$$V_{in}\delta T_s - (1 - \delta)(V_{in} - V_{C3} - V_0)T_s = 0.$$
 (8)

$$V_{C3} = \frac{V_{in}}{(1-\delta)} - V_0. \tag{9}$$

$$(V_{C2} + V_{C3})\delta T_s - V_0(1 - \delta)T_s = 0.$$
 (10)

where V_{in} is the source voltage (V); δ is the duty ratio of the converter; V_0 is the DC output voltage (V), and T_s is the switching period (s).

The above equations are used to derive the following voltage gain (M) equation 11 for the suggested converter.

$$M = \frac{V_0}{V_{in}} = \frac{\delta}{(1-\delta)^2} + \frac{\delta}{1-\delta}$$
 (11)

Thus, the proposed hybrid converter can yield relatively improved voltage gain as per eq. (11).

3. CONVERTER SIMULATION RESULTS AND DISCUSSION

The proposed hybrid converter is simulated MATLAB/Simulink environment, and the results are presented for the converter's performance validation. For simulation purposes, the switching frequency (f_s) of the converter is chosen as 15 kHz. The design of inductors and capacitors is carried out with consideration for minimizing ripples in inductor currents and capacitor voltages. A load resistor (R_0) of 290 Ω is connected at the load terminals. Table 1 lists the values of the parameters used in the simulation. The MOSFET switches S₁ and S₂ are triggered into conduction by the application of Pulse Width Modulated (PWM) signals as shown in Fig.6. Two separate DC sources each (Vin) of 12 V capacity are used to energize the conventional SEPIC and Cuk topologies of the hybrid structure. Figure 7 shows the source voltage (V_{in}). Figures 8 and 9 illustrate the input current waveforms of the conventional SEPIC and Cuk topologies. The switches S1 and S_2 are triggered into conduction at a duty factor δ of 0.6 to obtain an output voltage (V_0) of approximately 61.5 V and an output current Io of 0.98 A for the converter. The waveforms shown in Fig.10 and Fig.11 are those of output voltage (V_0) and output current (I_0) . The power switches and diodes are open-circuited when their cathode potentials are more positive than their anode potentials. During that time, a significant amount of reverse voltage may appear across the switches and diodes. In this work, the stress due to reverse potentials is found to be 96 V and 48 V, respectively, for the switches S₁ and S₂. The simulation analysis of the proposed converter has been carried out by selecting a typical range of switch duty factor (δ) from 0.6 to 0.85.

Table 1

Parameters and the values used in the simulation

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Parameters	Symbol	Value	
Source voltage to each converter	Vin	12 V	
	L_1, L_2, L_3, L_0	700 μH each	
Passive components	C_1	100 μF	
(Inductors & Capacitors)	C_2, C_3	3.3 µF each	
	C_0	1000 μF	
Resistance of the load	R_0	290 Ω	
Switching frequency	f_s	15 kHz	
Duty factor of the switches S ₁ & S ₂	δ	0.6 each	

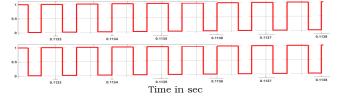


Fig. 6 - Triggering pulses for the switches S₁ and S₂.

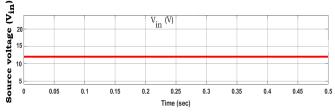


Fig. 7 – Source voltage (V_{in}) to the conventional SEPIC and Cuk. topologies.

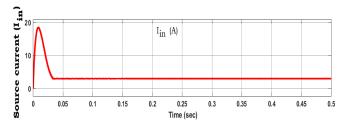


Fig. 8 – Source current (I_{in}) to the modified Cuk structure

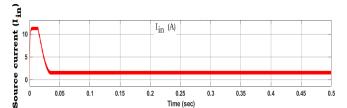


Fig. 9 – Source current (Iin) to the SEPIC topology.

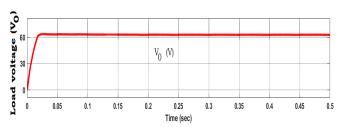


Fig. 10 – Load voltage (V₀) of hybrid DC-DC converter topology.

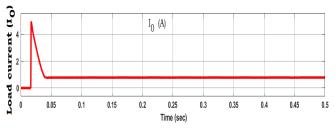


Fig. 11 - Load current (I₀) of hybrid DC-DC converter topology.

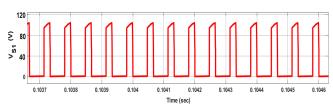


Fig. 12 - Reverse voltage stress (V_{S1}) across switch S₁

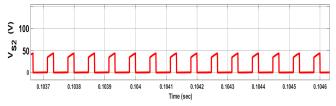


Fig. 13 – Reverse voltage stress (V_{S2}) across switch S₂.

4. EXPERIMENTAL SETUP AND ITS RESULTS

A prototype model of the proposed converter is developed, and its results are compared with those of the simulation for performance validation. The hardware model is shown in Fig. 14. The various hardware components and their specifications are listed in Table 2. The gate-to-source capacitance (V_{GS}) of a power MOSFET switch cannot be charged effectively using the dsPIC30F2010 microcontroller, as it is only capable of

producing an output signal at a low power level. So, a power electronic interface is required between the microcontroller and the switch. A gate driver circuit of the TLP250H category is used as an interface circuit for the MOSFET. The low-power controller output signal is fed to the driver circuit, which in turn produces high-current driving pulses for the gate terminals of both switches S₁ and S₂ at 60 % duty factor, as shown in Fig. 15. Both power switches have a switching frequency (f_s) of 15 kHz.

The conventional SEPIC and Cuk topologies, with a voltage boosting module in the prototype model, are energized by two separate DC sources ($V_{\rm in}$), consisting of batteries with a 12 V and 7.5 Ah capacity each. The input voltage ($V_{\rm in}$) and input current ($I_{\rm in}$) waveforms for the integrated converter structure are illustrated in Fig.16 for the Cuk topology and in Fig.17 for the SEPIC topology. The proposed hybrid converter, with a 60% duty factor, supplies power to a 60 W incandescent lamp load.

The corresponding load voltage (V₀) and load current (I₀) waveforms are shown in Fig. 18. Corresponding to a duty factor of 60%, the converter circulates a load current of 0.965 A through the load at a load voltage of 60.2 V. The reverse potential stresses appearing across the power switches are also measured. They are found to be 96 V and 48.4 V, respectively, as illustrated in Figs. 19 and 20. All the above waveforms are observed in a DSO (Digital Storage Oscilloscope). The simulation and hardware results are compared as shown in Table 3.

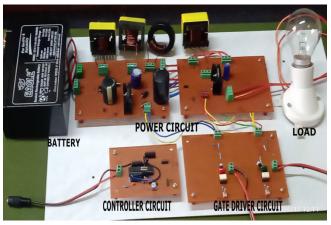


Fig. 14 – Experimental setup of the converter.

 $\label{eq:components} \textit{Table 2}$ Hardware components and specifications .

Components	Specifications
Two DC sources	12 V, 7.5 Ah each
MOSFET switches S ₁ & S ₂	2SK2645 N-Channel: 600 V, 9 A (each)
Diodes D ₁ , D ₂ , D ₃ , & D ₄	UF5408: 1000 V, 3 A (each)
Controller	dsPIC30F2010
MOSFET Driver	TLP250H
Inductors L ₁ , L ₂ , L ₃ , L ₀	1 mH each
Capacitor C ₁	100 μF
Capacitors C2, C3	10 μF each
Capacitor C ₀	1000 μF
Lamp load	60 W
Switching frequency (fs)	15 kHz
Duty cycle (δ) of MOSFET	0.6 each
switches S ₁ & S ₂	

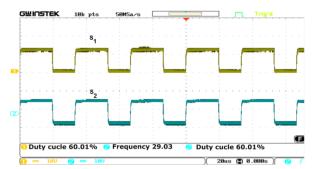


Fig. 15 – Triggering pulses applied to the switches S_1 and S_2 .

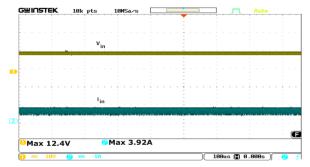


Fig. 16 – Input voltage ($V_{\rm in}$) and input current ($I_{\rm in}$) waveforms for the Cuk topology.

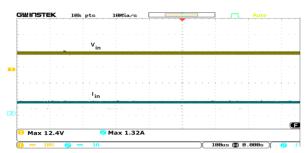


Fig. 17 – Input voltage (V_{in}) and input current (I_{in}) waveforms for the SEPIC configuration.

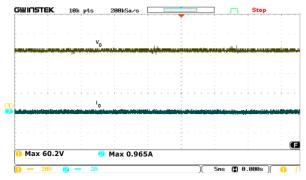
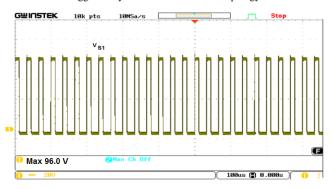


Fig. 18 – Output voltage (V₀) and output current (I₀) waveforms of the suggested hybrid DC-DC converter topology.



 $Fig.\ 19-Voltage\ stress\ (V_{S1})\ of\ switch\ S_1.$

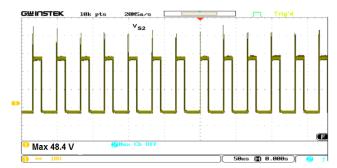


Fig. 20 - Voltage stress (V_{S2}) of switch S₂.

Table 3

Comparison of simulation and prototype model results of the suggested hybrid DC-DC converter

Parameters	Simulation results	Hardware results
Source voltage to each	12 V	12.3 V
converter (V _{in})		
Load voltage (V ₀)	61.6 V	60.2 V
Load current (I ₀)	0.98 A	0.965 A
Duty cycle (δ) of the switches	0.6 each	0.6 each
$S_1 \& S_2$		
Switch voltage stress (V _{S1} &	96V & 48V	96 V & 48.4V
V_{S2})		

5. CONCLUSIONS

The work presented in this paper interprets the operating modes of the projected non-isolated hybrid high-gain DC-DC power electronic converter topology during steady state. The integrated converter structure, featuring two 12 V DC sources and a duty cycle of 0.6 at a switching frequency of 15 kHz, is simulated in the MATLAB/SIMULINK platform. An experimental setup of the converter is also developed using low-power devices, and its performance is compared with that of the simulation model. The parameters used in the hardware model have the same values as those used in the simulation setup for ease of comparison of results. The hybrid converter configuration achieves a relatively high voltage gain at a low duty ratio and operates in a nonzero inductor current mode, utilizing a simple PWM control technique. Further, lower voltage stress is observed on semiconductor-based components employed in the topology. The unregulated low DC voltages produced by solar PV sources can be regulated and stepped up to higher voltage levels using the proposed topology. Hence, the projected converter topology can be better employed in electrical power generation using renewable energy sources and in electric vehicle technology.

CREDIT AUTHORSHIP CONTRIBUTION STATEMENT

Author_1: Methodology; Conceptualization; Investigation; Writing – original draft; Validation.

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