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A DOUBLE SWITCH INTEGRATED HIGH-GAIN QUADRATIC BOOST CONVERTER FOR ELECTRIC VEHICLE APPLICATIONS

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Keywords: High-gain converter; Light electric vehicles (LEVs); Active switched capacitor; Voltage multiplier cell (VMC); Quadratic boost structure.

The rapid development of electric vehicles in the automotive industry opens the door for the development of DC-DC converters. This paper proposes a high-gain DC-DC converter with a lower part count for light electric vehicle (LEV) applications. When the converters are cascaded for maximum gain, a topology change is recommended that involves the integration of a voltage multiplier and a switching capacitor with a quadratic boost structure. A remarkable 496 is offered by this converter. Additionally, the theoretical portion of this work covers the 496 performance of the presented converter. Furthermore, MATLAB/Simulink is utilized to simulate the proposed configuration, which confirms the theoretical findings, and a 100 W laboratory prototype of the same is fabricated and tested to verify the performance of the presented converter.

1. INTRODUCTION

A desire for greener and energy-efficient modes of transportation has led to an innovative transformation in the automobile industry with the emergence of electric vehicles (EVs). High-gain converters are an essential part of modern power electronic systems that are integrated into EVs to improve their efficiency and performance. A specialized power electronic system with 496 voltage levels from battery packs to match the voltage levels between components, such as the battery and the motor drive system. To effectuate such a form of mobility often requires familiarity with global charging standards, battery charging infrastructures, and impending advancements in on-board chargers (OBCs) with effective power conversion circuits [1–3]. Unlike the classical boost converter in [4], several other converters with high boosting capabilities have now been reported in the literature to overcome the inefficient extreme duty cycle operation of the traditional boost topology. These high-gain structures can be categorized into isolated or non-isolated depending on the applications.

Non-isolated DC converters are beneficial in a range of applications where high voltage is needed but isolation is not necessary [5,6]. Certain applications require isolated converters, which are used in conjunction with high-frequency transformers to provide isolation [7,8]. Yet it comes with drawbacks such as a larger size and leakage inductance. Also, a wide variety of voltage boosting techniques, such as cascading [9] and interleaving [10], are employed in many applications. Furthermore, the concept of using coupled inductors with a hybrid combination of two converters to achieve high voltage gain has gained popularity recently to reduce voltage issues on power switches [11–13]. However, the coupled inductor's leaking inductances are the source of increased electromagnetic interference (EMI) noise, static and dynamic losses, and high voltage spikes over power switches. Despite the numerous challenges in implementing coupled inductors to achieve high voltage gain, some researchers have nonetheless constructed power conversion circuits with lower static and dynamic losses [14].

Regenerative snubber circuitries and the design of clamped circuits are reviewed in [15,16] as a further strategy to address these issues; however, doing so adds complexities as well as cost to the power circuits. On the other hand, non-coupled inductor circuits avoid these downsides and offer additional merits, including low cost, small size, light weight, minimal circuit intricacies, and are also feasible for EV charging solutions. On top of that, several other voltage boosting designs such as voltage lifters [17,18], quadratic boosters [19], active switched inductor (SL) networks [20], active switched capacitors structure (SC) [21], integration of SL-SC structure [22], SL network coupled voltage multiplier cells [23], expandable gain schematics [24] and other configurations [25,26]. The concept of using multipliers and n-boosting stages to maximize voltage gain suffers from a larger number of circuit parts, which increases the overall cost and size.

Also, opportunities to improve the performance of high-step-up converters remain prevalent today. Therefore, this article reveals a new structure of a DC-DC converter that integrates a quadratic boost structure with VMC and SC networks to enhance voltage gain with reduced stress over fewer circuit parts. Besides, an in-depth description of the recently developed converter architecture with its functional modes, stability, and efficiency analysis is given, along with Simulink and laboratory findings to support the study.

2. ANALYSIS OF OPERATING MODES

Figure 1 portrays the circuit of the proposed converter. To increase the gain, a VMC and SC circuit are integrated with a QBC structure. As the two switches operate simultaneously, the same gating pulse is applied to switches S_{w1} and S_{w2}. The proposed converter comprises four diodes, two switches, five capacitors, and two inductors. This analysis assumes all elements are ideal, the capacitor is large, all inductors have the same inductance, and the converter operates in CCM. Based on the operation of the switches S_{w1} and S_{w2}, there are two operating modes.

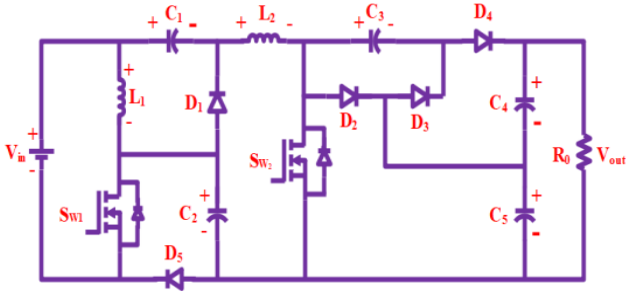

Fig. 1 – proposed converter circuit.

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2.1 MODE 1 OPERATION

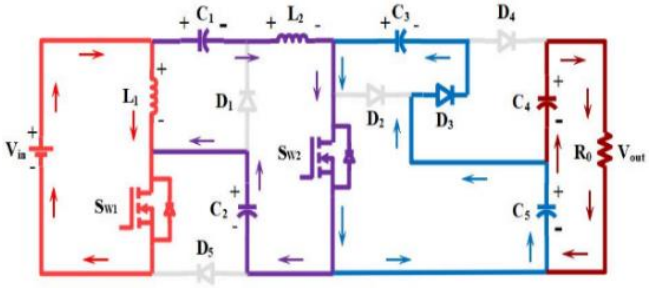

Fig. 2 – Converter equivalent circuit in Mode 1.

Figure 2 portrays the converter equivalent circuit in Mode 1, in which switches S_{w1} and S_{w2} are in the ON position. In this mode, diode 3 is ON while the remaining diodes are in the OFF state. This mode involves charging the inductors L_1 and L_2, capacitor C_1, and discharging the remaining capacitors. Equations (1) to (4) give the voltage and current relations in M 1.

$$V_{in} - V_{L1} = 0, \tag{1}$$

$$V_{in} + V_{C1} - V_{L2} + V_{C2} = 0, \tag{2}$$

$$V_{C3} + V_{C5} = 0, \tag{3}$$

$$V_{C4} + V_{C5} = V_0. \tag{4}$$

2.2 MODE 2 OPERATION

Figure 3 shows the conduction diagram in Mode 2, where switches S_{w1} and S_{w2} are in the OFF state. Diode D_3 is reverse-biased while the remaining diodes are conducting in this mode. The discharging of inductors L_1, L_2, and capacitor C_1 takes place in this mode while the remaining capacitors are charged. The current and voltage relations of this mode are given in eq. (5) to (9).

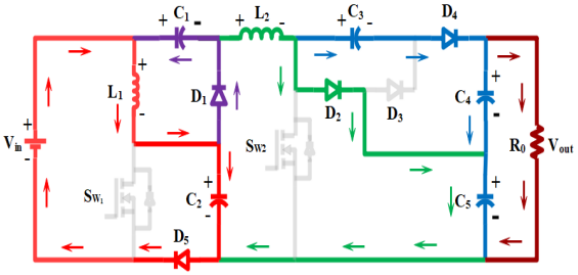

Fig. 3 – Converter equivalent circuit in Mode 2.

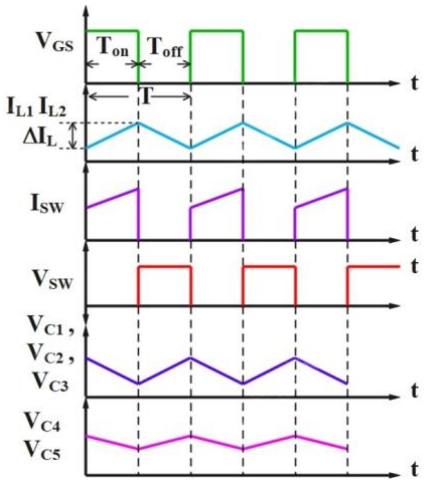

Fig. 4 – Chief operating waveforms.

$$V_{C1} + V_{L1} = 0, \tag{5}$$

$$V_{L1} = V_{in} - V_{C2}, \tag{6}$$

$$V_{C3} = -V_{C4}, \tag{7}$$

$$V_{L2} = V_{C2} - V_{C5}, \tag{}$$

$$V_{L2} = V_{C2} - V_{C3} - V_0. \tag{9}$$

Figure 4 portrays the chief operating waveforms of the converter proposed.

2.3 VOLTAGE GAIN COMPUTATION

The volt-second balance principle is applied to inductor L_1 to obtain:

$$V_{L1(mode\ 1)}D + V_{L1(mode\ 2)}(1 - D) = 0. \tag{10}$$

By using eq. (1) and (6) in (10), we get:

$$V_{in}D + (V_{in} - V_{C2})(1 - D) = 0. \tag{11}$$

By simplifying eq. (11), we get capacitor voltage V_{C2} as mentioned in (12).

$$V_{C2} = \frac{V_{in}}{(1-D)}. \tag{12}$$

By using eq. (1) and (5) in (10), and simplifying, we get capacitor voltage V_{C1} as:

$$V_{C1} = \frac{V_{in}D}{(1-D)}. \tag{13}$$

The volt-second balance principle, when applied to inductor L_2, yields:

$$V_{L2(mode\ 1)}D + V_{L2(mode\ 2)}(1 - D) = 0. \tag{14}$$

By using eq. (2), (8) and (9) in (14), and simplifying, we get capacitor voltages V_{C3}, V_{C4}, and V_{C5} as:

$$V_{C3} = V_{C4} = V_{C5} = \frac{V_{in}(1+D)}{(1-D)^2}. \tag{15}$$

From eq. (4) and (15), the voltage gain is:

$$\frac{V_0}{V_{in}} = \frac{2V_{in}(1+D)}{(1-D)^2}. \tag{16}$$

2.4 VOLTAGE STRESS ON POWER DEVICES

The power device voltage stress indicates its voltage-blocking capability during OFF mode and is specified by eq (17) and (18):

$$V_{S1} = \frac{V_{in}}{1-D}. \tag{17}$$

$$V_{S2} = \frac{(1+D)V_{in}}{(1-D)^2}. \tag{18}$$

$$V_{D1} = V_{D5} = \frac{V_{in}}{1-D}. \tag{19}$$

$$V_{D2} = V_{D3} = V_{D4} = \frac{V_{in}(1+D)}{(1-D)^2}. \tag{20}$$

2.5 COMPONENTS SELECTION

2.5.1 INDUCTOR SELECTION

The inductor is chosen based on the current ripple through it. From eq. (1):

$$V_{L1} = L_1 \frac{\mathrm{d}i_{L1}}{\mathrm{d}t} = V_{in}, \tag{21}$$

$$L_1 = \frac{DV_{in}}{\Delta I_{L1} f}, \tag{22}$$

where ΔI_{L1} is the current ripple of inductor L_1. From eq. (8):

$$V_{L2} = L_2 \frac{\mathrm{d}i_{L2}}{\mathrm{d}t} = V_{C2} - V_{C5}. \quad (23)$$

$$L_2 = \frac{2DV_{in}}{(1-D)\Delta I_{L2} f}, \quad (24)$$

where f represents the switching frequency. Equations (22) and (24) yield the designed value of inductance.

2.5.2 CAPACITOR SELECTION

The ON mode and OFF mode capacitor current equations, when applied with the capacitor charge balance principle, yield the capacitor formula as stated in equations (25) and (26).

$$C_1 = C_2 = \frac{(1+7D-5D^2)I_0}{(1-D)f\Delta V_{C1}}, \quad (25)$$

$$C_3 = C_4 = C_5 = \frac{I_0 D}{\Delta V_{C5} f}, \quad (26)$$

where ΔV_c indicates the ripple voltage across the capacitor.

3. COMPARATIVE ASSESSMENT OF PROPOSED CONVERTER

In this section, the recommended converter is contrasted with other new converters. This comparison considers the count of active and passive components used, the gain obtained, and the switch voltage stress and is presented in Table 1. The suggested converter has the same number of components as the converters from [12] and [26]. Nonetheless, the gain of the proposed converter is high. Despite having a lower component count, the converter presented in [24] outputs a gain of 18, which is significantly lower than the 90 of the proposed converters at a duty cycle of 0.8. The converter presented in [20] has 18 components, compared with 14 in the proposed converter. In addition, the proposed converter yields a gain of 90 for D = 0.8 as compared to the gain of 39 in [20]. Figure 5 shows that, based on the relationship between duty ratio and gain across different converters, the suggested converter gain is extremely high.

Table 1

Comparison of the suggested converter with competing topologies.

Topology	Proposed Converter	[12]	[20]	[24]	[26]
Voltage Gain	$\frac{2(1+D)}{(1-D)^2}$	$\frac{5+D}{1-D}$	$\frac{7+D}{1-D}$	$\frac{2(1+D)}{1-D}$	$\frac{3-D}{(1-D)^2}$
Switch	2	2	2	1	2
Diode	5	5	7	6	5
L	2	2	4	2	2
C	5	5	5	3	5
Max. Voltage Stress on Switch	$V_{S1} = \frac{V_{in}}{1-D}$ $V_{S2} = \frac{(1+D)V_{in}}{(1-D)^2}$	$\frac{V_{in}}{1-D}$	V_{in}	$\frac{(1+D)V_{in}}{1-D}$	$\frac{(3-D)V_{in}}{4(1-D)^2}$
Voltage Stress on Diode	$V_{D1} = V_{D5} = \frac{V_{in}}{1-D}$ $V_{D2-4} = \frac{V_{in}(1+D)}{(1-D)^2}$	$\frac{2V_{in}}{1-D}$	$V_{D1-4} = \frac{V_{in}}{1-D}$ $V_{D5-7} = \frac{4V_{in}}{1-D}$	$\frac{(1+D)V_{in}}{1-D}$	$V_{D1} = \frac{V_{in}}{1-D}$ $V_{D2-4} = \frac{(3-D)V_{in}}{4(1-D)^2}$

4. DISCUSSIONS ON SIMULATION AND EXPERIMENTAL RESULTS

Simulations are done in MATLAB to determine the converter's functionality, and a developed prototype model verifies the simulation results. Table 2 presents the parameter values utilized in the simulation.

Table2

Parameter values in simulation.

Parameters	Value
Supply Voltage (V_{in})	24 V
Output Voltage (V_{out})	185 V
Output Power (P_{out})	100 W
Switching Frequency	20 kHz
Capacitors (C_1)	100 µF
Capacitors (C_2, C_3 C_4 and C_5)	220 µF
Inductors (L_1 and L_2)	560 µH, 4.6 mH

5. CLOSED LOOP SIMULATION RESULTS

To attain a voltage output of 200 V and maintain the same under varying conditions, a proportional-integral controller is employed in simulation. Figure 8 exhibits the output voltage waveform of the suggested converter under closed-loop control. It takes 0.3 seconds to reach the target output voltage of 200 V. The waveform also suggests very little voltage ripple.

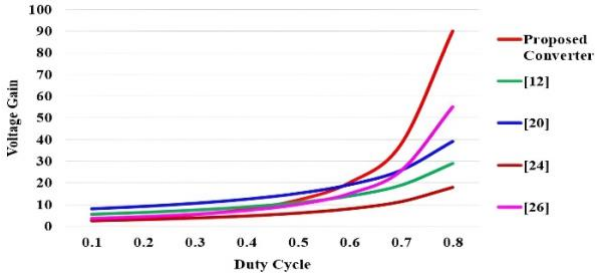

Fig. 5 – Gain *vs* duty ratio plot for various converters.

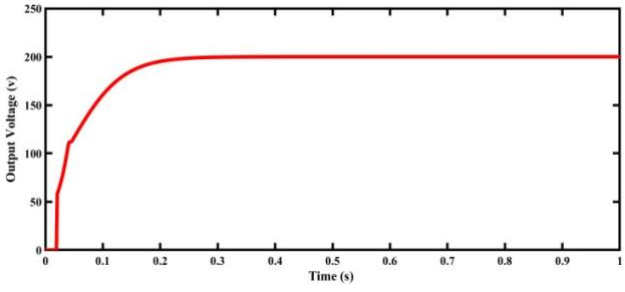

Fig. 6 – Output voltage waveform for closed-loop control.

CASE 1: REFERENCE VOLTAGE VARIATION

The behaviour of the converter load voltage in response to variations in the reference voltage is analyzed in this scenario. From t = 0 s to 0.5 s, the reference voltage is

maintained at 240 V. At t = 0.5 s, it is decreased to 200 V, and at t = 1 s, it is raised to 280 V. The corresponding changes in the load voltage and load power, in accordance with these variations in the reference voltage, are depicted in Fig. 7.

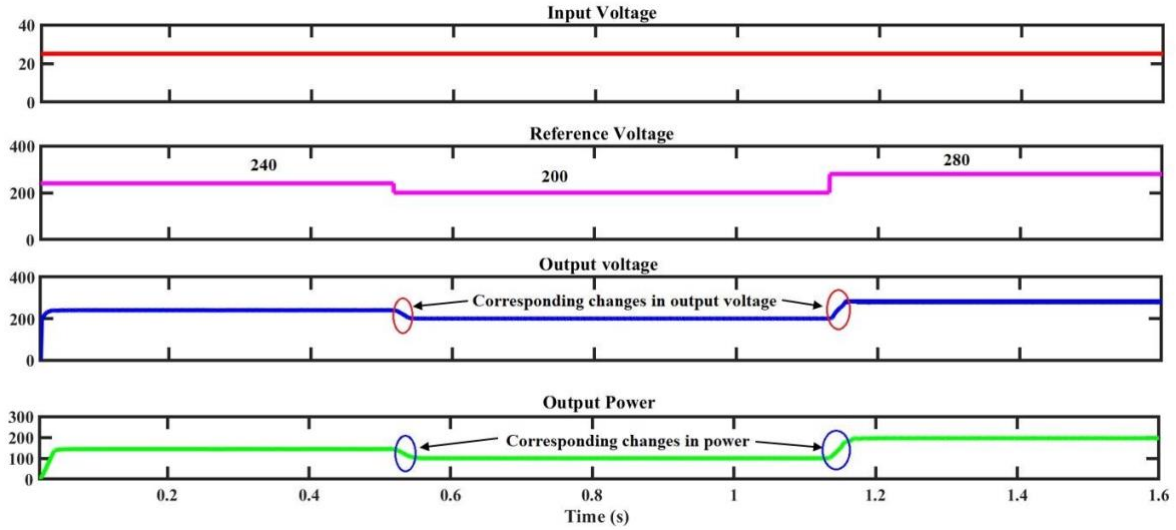

Fig. 7 – Performance of the proposed converter under reference voltage variation.

CASE 2: LOAD VARIATION

In the simulation analysis, sudden load changes are applied to the converter to analyze the corresponding effects on the output power, output current, and output voltage. At t = 0.5 s, a 50% load is applied, resulting in small changes in the output voltage. The output current gradually decreases to 0.3 A, and the corresponding output power decreases to 50 W. At t = 1 s, a 30% load is applied, resulting in small changes in the output current to 0.2 A, and the output power drops below 50 W. Finally, at t = 1.5 seconds, a sudden 100% load is applied, causing the current to gradually increase to 0.5 A, resulting in a power flow of 100 W in the converter. These changes are depicted in Fig. 10.

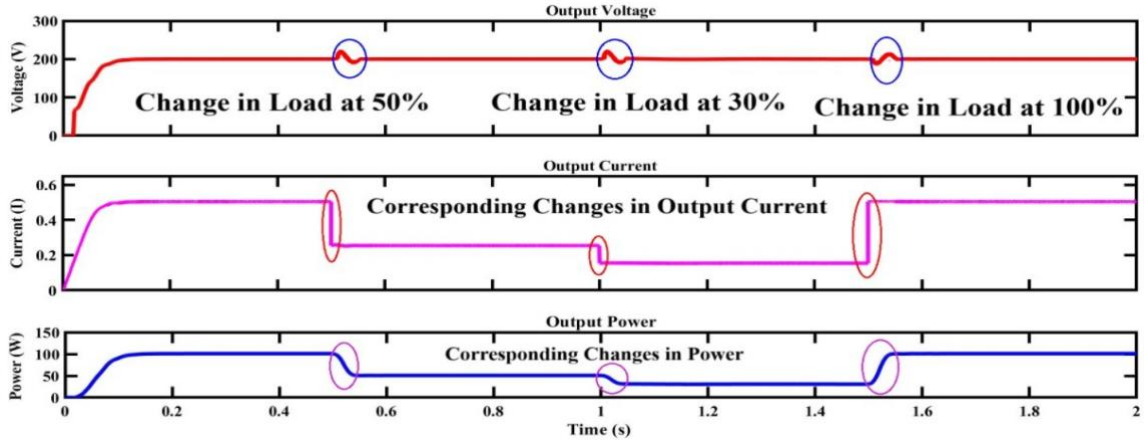

Fig. 8 – Performance of the proposed converter under load variation.

5. HARDWARE OUTPUTS AND DISCUSSIONS

By building a prototype in the lab, the effectiveness of the suggested converter is evaluated. Figure 11 portrays the hardware model developed in the laboratory for testing. The L_1 and L_2 values are chosen such that the converter current is continuous. Table 3 displays the hardware parameters.

Table 3

Hardware parameters

Components	Part Number	Rating
Switches S_{W1}, S_{W2}	SGL160N60UFD Ultrafast IGBT	600 V, 80 A
Diode D_1 – D_5	MUR3060PT Ultrafast Rectifier	600 V, 30 A
Inductor L_1 – L_2	Toroidal Core	560 µH, 4.6 mH
Capacitors C1	SA1112CMEKB0	100 µF, 160 V
C2	SA2212CM3HB0	220 µF, 220V
C3, C4, C5	SA2212HMTHB0	220 µF, 500V

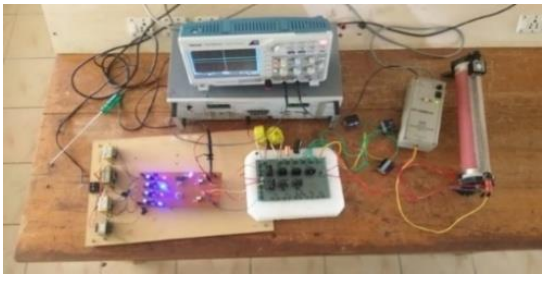

Fig. 9 – Hardware prototype model.

The gating pulse and output voltage waveform are shown in Fig. 12. Figures 13 and 14 display the currents of inductor L_1 and L_2, respectively. The voltage across the diodes is revealed in Figs. 15 to 19. From the figures, the voltage stress across diodes 1 and 5 is less than half of the output voltage, and for diodes 2, 3, and 4, it is half of the output voltage.

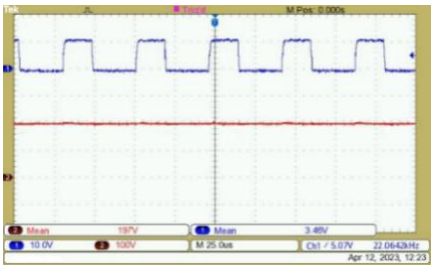

Fig.10 – Gating pulse and output voltage.

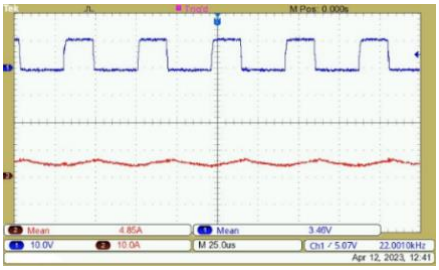

Fig. 11 – Current through $L1$ waveform.

Fig. 12 – Current through L_2.

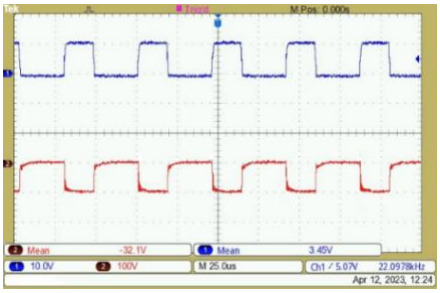

Fig. 13 – Voltage across D_1.

Fig. 14 – Voltage across D_2.

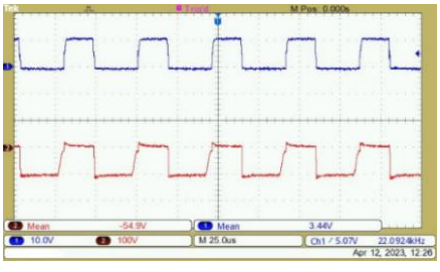

Fig. 15 – Voltage across D_3.

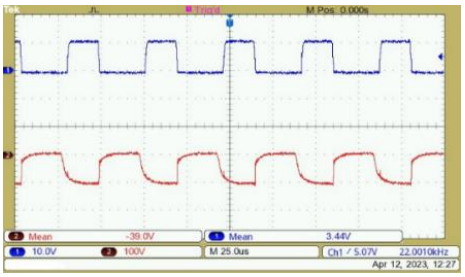

Fig.16 – Voltage across D_4.

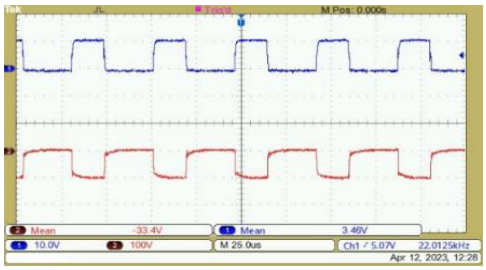

Fig. 17 – Voltage across D_5.

6. CONCLUSION

A newly modified double switch DC-DC converter featuring an integration of a voltage multiplier and a switched capacitor with a quadratic boost structure is introduced in this article. Numerous advantages of the presented converter include its ability to provide high voltage gain without the need for magnetic coupling, low conduction losses, universal input voltage, and low stress on semiconductor devices. Thus, it is a great, affordable option for battery-operated vehicles because of these attributes.

The integrated concept to derive the high-gain converter offers additional merits like enhanced voltage conversion ratio with reduced component count and power conversion efficiency of 95%. Besides, a detailed discussion on the different operating conditions of the proposed converter is presented along with adequate mathematical expressions.

Additionally, to justify the best features of the proposed high-gain structure, a detailed comparison is made among various step-up configurations reported in the literature. Finally, an experimental setup of the modelled converter with a rated power of 100 W is realized and tested in a laboratory to confirm theoretical ideas, Simulink outcomes, overall performances, and its feasibility.

CREDIT AUTHORSHIP CONTRIBUTION

Gnanavadivel Jothimani: main conceptual ideas and proof outline
Kalarathi Mahalingam: Design, simulation, and manuscript preparation
Prakash Karuppasamy: Hardware implementation

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