Rev. Roum. Sci. Techn.– Électrotechn. et Énerg.
Vol. **70**, *3*, pp. 355–360, Bucarest, 2025

HYBRID PNN-PPN 10T SRAM AND LEAKAGE CONTROL TRANSISTORS FOR LEAKAGE REDUCTION IN VLSI

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Keywords: Leakage current transistors; Integrated circuits; CADENCE Virtuoso; Hybrid PNN-PPN 10T SRAM; Very large-scale integration (VLSI).

Leakage power, defined as the unwanted current flow when a transistor is in the OFF state, significantly impacts the power consumption and performance of VLSI designs, particularly during standby modes. Existing methods to reduce leakage power in SRAM cells often fail to strike a balance between power efficiency, stability, and performance under varying operational conditions. This study proposes a hybrid PNN-PPN 10T SRAM configuration incorporating leakage control transistors (LCTs) to mitigate leakage. The innovative design combines elements of PNN and PPN architectures, strategically integrating additional PMOS and NMOS transistors to create high-impedance paths between V_{dd} and ground. Using the CADENCE Virtuoso tool for circuit design and the Spectre simulator for performance evaluation, the proposed hybrid SRAM cell demonstrates significant improvements in key performance metrics. Results show a notable reduction in dynamic and leakage power consumption, enhanced speed with lower delay, and a reduced power-delay product (PDP) across varying voltage levels. Specifically, the inclusion of LCTs results in a substantial decrease in leakage power and delay, thereby contributing to overall energy efficiency and faster operation. Static noise margin (SNM) evaluation under read, write, and hold conditions further validates the robustness of the proposed design, ensuring reliable data retention and minimal leakage during standby modes. The study concludes that the proposed hybrid PNN-PPN 10T SRAM with LCTs offers a promising solution for low-power, high-performance memory applications, addressing the critical challenge of leakage power in advanced semiconductor technologies.

1. INTRODUCTION

In the late 1970s, very-large-scale integration (VLSI) is a technique developed that fabricates Integrated Circuits (ICs) by embedding millions of transistors onto a single silicon chip. ICs are classified into four groups based on the quantity of transistors or gates they contain: SSI, MSI, LSI, and VLSI. In VLSI, CMOS technology is favored because of its strong noise resilience and low static power consumption [1]. Most integrated circuits had limited functions before the development of VLSI. The System-on-Chip (SoC) architecture, made possible by VLSI, allows several functionalities to be integrated into a single chip. Due to this progress, handheld devices now feature smaller circuit boards, faster operating speeds, reduced power consumption, and more affordable hardware. In the era of Internet of Things (IoT), where extended battery life and fast memory are essential, VLSI technology plays a crucial role in meeting these demands. Smart infrastructure, including buildings, cars, homes, and agricultural systems, heavily relies on low-power IoT sensor nodes [2]. As IoT applications continue to proliferate, the need for power-efficient technologies becomes increasingly vital for seamless daily experiences. These technologies often involve numerous battery-operated, portable devices interconnected through sensor nodes [3].

The information and instructions needed for processing are stored in memory. The basic building block of a memory array is a memory cell, which is organized in rows and columns and is uniquely addressed. These MOS transistor-built cells are used to store binary data, which is represented by the numbers 0 or 1. As short-term memory, random-access memory (RAM) stores data and applications that the CPU actively uses in real-time. Data can be read, written, and erased indefinitely with it. Fast data retrieval from RAM enables the CPU to handle multiple tasks simultaneously. Modern CPUs have undergone substantial speed advancements, while RAM has primarily been enhanced to increase storage capacity and reduce latency. To facilitate on-chip data processing and improve computational speed, energy-efficient cache memory remains essential. Such , cache memory, typically constructed using SRAM, must exhibit improved speed, performance, and reliability to meet the evolving demands of IoT-driven environments [4].

SRAM, a type of semiconductor memory extensively used in microprocessors, general computer systems, and various electronic applications, differs from its dynamic counterpart in its static data storage nature, eliminating the need for frequent refreshing [5]. This type of memory is volatile, meaning data is lost when power is cut off. SRAM's distinct feature lies in its ability to store data without dynamic refreshing, enabling unrestricted read and write access regardless of the sequence in which memory locations are accessed [6]. SRAM stands out as the preferred choice for applications requiring high-speed and random access due to its versatile data modification capabilities, setting it apart from other memory types.

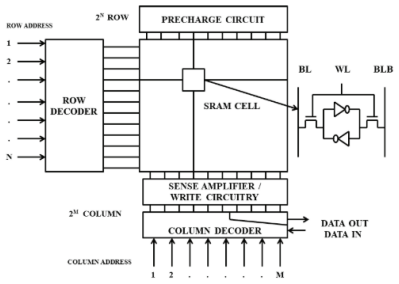

Fig. 1 – Architecture of SRAM.

The sensing amplifier, precharge circuit, row/column decoder, and SRAM cell are the primary components of the SRAM architecture, as illustrated in Fig. 1. The decoder translates binary addresses into unary addresses to select specific memory locations. Word Line (WL) can be enabled by using a row and column decoder. SRAM cells store binary information using bistable latching circuitry, typically utilizing six MOSFETs. Sense amplifiers detect and amplify signals from bit lines, while the precharge circuit precharges bit lines (BL and BLB) before read/write operations. Write driver circuits discharge bit lines during write operations, controlled by write enable signals. Decoders decode addresses to enable specific rows or columns in the memory array, facilitating read and write operations.

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DOI: 10.59277/RRST-EE.2025.70.3.12

Different types of SRAM cells utilize varying numbers of transistors, ranging from 4 to 10 or more, to store a single bit of data. At its core, the SRAM memory cell comprises four transistors arranged as two cross-coupled inverters representing logical "0" and "1" states. When the number of transistors increases in the SRAM cell, a separate read circuit is often employed. There are three main modes of operation for the SRAM cell: write, read, and standby (or hold).

Additional transistors are introduced to regulate access during read and write operations. With its intrinsic properties, including speed, random access capabilities, and operational non-volatility, SRAM is widely used in critical computing applications where rapid data modification and retrieval are essential. Ongoing developments in semiconductor technology aim to enhance SRAM designs, ensuring optimal performance and energy efficiency in dynamic electronic systems [7]. During operation, various parameters can be measured to assess performance, including power consumption, power delay product, delay, and stability.

A critical consideration in SRAM design, due to its impact on electronic system performance and energy efficiency, is power dissipation [8]. Three primary sources contribute to power dissipation in SRAM: dynamic power, short circuit power, and static or leakage power [9]. Dynamic power dissipation occurs primarily during read and write operations due to logic level switching, leading to energy consumption as load capacitance is charged and discharged [10]. This type of power dissipation is directly related to the dynamic nature of SRAM operations. Additionally, SRAM circuits may experience static or leakage power dissipation when idle, with OFF transistors within the SRAM cells exhibiting subthreshold currents and leakage currents despite the absence of an applied gate voltage [11].

When considering low-power design considerations, excessive power dissipation can notably elevate total power consumption. This is particularly evident during the simultaneous operation of the pull-up and pull-down networks, which leads to short-circuit power dissipation [12]. This phenomenon occurs due to the fluctuating response of the output to changes in input signals. The simultaneous activation of both networks during specific transitions results in increased power dissipation, thereby impacting the overall energy efficiency of the SRAM.

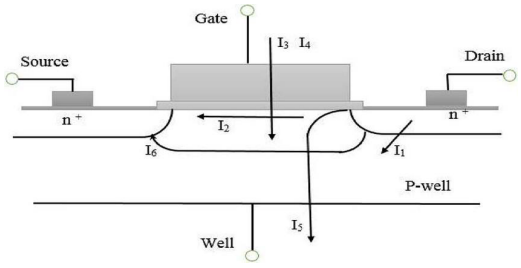

Fig. 2 – Leakage current mechanism.

Leakage power in SRAM refers to the power consumed by the transistors in the memory cells even when they are not actively performing any operations [13]. This leakage current occurs due to various factors, including junction leakage, subthreshold leakage, and gate oxide leakage. Despite no data being accessed or manipulated, the transistors still allow a small amount of current to flow, leading to power dissipation. Figure 2 shows the diagram of leakage current in a transistor circuit.

I_1 is the reverse-bias leakage current of a PN junction.

I_2 = subthreshold leakage current

I_3 = oxide tunneling current

I_4= hot-carrier injection-related gate current

I_5 is GIDL-Gate-Induced Drain Leakage.

I_6= channel punch through current.

Static power, also known as leakage power, arises from subthreshold currents that persist without an applied gate voltage and leakage currents that pass-through transistors, particularly in their off state. When SRAM is inactive, leakage power becomes a significant concern as all power consumed during this period is essentially considered leakage, diminishing energy efficiency. Mitigating leakage power in SRAM necessitates leveraging advanced fabrication technology, specialized transistors, and optimizations in circuit design.

$$P_{dynamics} = \alpha C_L V^2{}_{dd} f. \quad (1)$$

$P_{dynamics}$ is the Dynamic power, α is the Activity factor, $C_L$is the load capacitance, V_{dd} is the supply voltage, f is the operating frequency.

$$P_{static} = I_{leak} V_{dd}. \quad (2)$$

P_{static} is the static power, $I_{leak}$is the leakage current, $V_{dd}$is the supply voltage.

$$P_{short} = I_{sc} V_{dd}. \quad (3)$$

P_{short} is the short circuit current, $I_{sc}$is the short circuit current, $V_{dd}$is the supply voltage

$$P_{total} = P_{dynamics} + P_{static}. \quad (4)$$

$$P_{total} = (P_{short} + P_{switch}) + P_{static}. \quad (5)$$

$$P_{total} = I_{sc} V_{dd} + \alpha C_L V^2{}_{dd} f + I_{leak}. \quad (6)$$

Dynamic power dissipation occurs during circuit operation and consists of short-circuit and switching power [14]. The process of charging and discharging node capacitances generates switching power, whereas short-circuit power arises from slow input changes [15]. Gate delays contribute to glitching power dissipation, which occurs when the circuit output briefly becomes "1" due to input state changes, resulting in increased power dissipation [16].

An exclusive master-slave flip-flop topology is proposed using clocked complementary metal-oxide-semiconductor (CMOS) logic, which minimizes the total device count and the number of clocked devices [17]. A higher-order multifunction filter design is proposed, specifically low pass (LP), high pass (HP), and bandpass (BP) filters using a current differencing buffered amplifier (CDBA) as an active element. A general voltage transfer function is observed in four admittance terms to facilitate the fifth-order filter function [18].

Leakage power in SRAM presents formidable challenges for the development of low-power VLSI devices, demanding effective solutions to ensure power efficiency and prolong battery life, particularly in the context of escalating demand for portable devices. This research delves into the critical realm of SRAM leakage reduction by proposing a novel approach that integrates hybrid combination and LCT techniques. Through the integration of LCT and hybrid combination methods, the objective is to minimize leakage

currents and decrease static power dissipation during idle states. It underscores the ongoing need to balance the pursuit of enhanced functionality and performance in semiconductor technology with a concerted focus on mitigating power dissipation for sustainable energy efficiency. The research work presents significant contributions in the domain of SRAM circuit design, focusing on enhancing its efficiency and performance:

- To propose a novel hybrid PNN-PPN 10T SRAM architecture with LCTs to address leakage issues in semiconductor memory design.
- To develop innovative transistor configurations and hybrid architectures to optimize SRAM cell performance, energy efficiency, and reliability during standby modes.
- To conduct detailed simulations and waveform analyses to validate the efficiency of the proposed hybrid SRAM cell, demonstrating significant improvements in dynamic power consumption, leakage power reduction, delay minimization, and PDP enhancement.
- To evaluate performance metrics including static noise margin (SNM) under various operational conditions, showcasing the robustness and reliability of the proposed SRAM architecture against noise and disturbances.
- To provide comprehensive insights into the design and optimization of low-power VLSI circuits, contributing to advancements in energy-efficient semiconductor memory applications.

These contributions collectively address key challenges in SRAM design, paving the way for more energy-efficient and reliable memory solutions.

The rest of the paper is structured as it follows: section 2 presents the materials and methods. Section 3 is focused on results and discussion, and section 4 provides the conclusion.

2. MATERIALS AND METHODS

Leakage current, a critical concern in semiconductor design, refers to the undesired flow of electric charge through a transistor when it should ideally be in the OFF state. This leakage current significantly impact the power consumption and overall performance of integrated circuits, especially during standby modes where minimizing power consumption is crucial. In PNN and PPN SRAM cells, reducing leakage current is essential for improving energy efficiency and extending battery life in portable devices. The study aims to address the critical issue of leakage current in SRAM cells by employing innovative transistor configurations and hybrid architectures. The proposed research suggests a hybrid PNN-PPN 10T SRAM configuration designed to mitigate leakage current through the incorporation of Leakage Control Transistors (LCTs). By incorporating both types of transistors, the design leverages the strengths of each architecture to create an optimized SRAM cell with improved leakage control. This method enhances power efficiency while simultaneously improving the reliability and overall performance of semiconductor devices in low-power operation modes.

2.1. HYBRID PNN-PPN 10T SRAM

The hybrid PNN-PPN 10T SRAM architecture combines elements from both PNN and PPN structures to create a robust memory cell design. At its core, this architecture features ten transistors organized to facilitate efficient read and write operations while maintaining data integrity during standby modes. The SRAM cell comprises two cross-coupled inverters formed by pairs of complementary transistors, along with access transistors that enable connectivity between storage nodes and bit lines. During write operations, the activation of specific control lines allows data to be written into the cell by controlling the flow of charge between the storage nodes and the bit lines. Similarly, in read operations, the data stored is retrieved by sensing the levels of voltage on the bit lines, facilitated by the activation of appropriate control lines.

The hybrid PNN-PPN 10T SRAM architecture encounters several significant limitations that demand attention. Leakage currents, particularly troublesome during standby modes, significantly impact the energy efficiency and lifespan of portable devices. Additionally, the architecture's stability and reliability suffer across varying operational conditions such as process, voltage, and temperature. In high-density and high-speed applications, the system is prone to read and write disturbances, heightened by its sensitivity to noise and fluctuations, which could compromise data integrity and overall performance. Furthermore, the architecture's potential for achieving optimal leakage current reduction is hindered, limiting its suitability for energy-efficient memory applications.

To effectively address these shortcomings, integrating LCTs into the hybrid PNN-PPN 10T SRAM architecture is imperative. LCTs offer a valuable solution by establishing a higher impedance path between the supply voltage and ground, thereby significantly diminishing leakage current during standby modes and bolstering stability and reliability.

2.2. PROPOSED HYBRID PNN-PPN 10T SRAM WITH LCT

The proposed framework is designed to mitigate leakage currents and enhance energy efficiency, which is particularly important for low-power applications. The 10T SRAM cell incorporates ten transistors: four PMOS (P1-P3) and six NMOS (N1-N7). The core of the SRAM cell comprises the typical 6T configuration, including cross-coupled inverters formed by P1, P2, N1, and N2, which establish the storage nodes Q and QB, as depicted in Fig. 3. When the bit lines (BL and BLB) are enabled, access transistors N3 and N4 link the storage nodes to them.

The innovative aspect of this design lies in the use of additional transistors (P3, N5, N6, N7) and the implementation of an LCT. These components are strategically placed to manage and minimize leakage currents. N5 is positioned between the cross-coupled inverters and the access transistors. When the cell is not being accessed (WL is low), N5 is turned off, effectively isolating the storage nodes from the bit lines. This isolation prevents leakage paths from forming through the access transistors and bit lines, significantly reducing the leakage current.

During a write operation, the WL is activated (WL is high), which turns on the access transistors N3 and N4. The BL and BLB are driven to the desired values to write data into the storage nodes. When WL is high, N5 is turned on, connecting the storage nodes to the bit lines. The write operation is controlled in such a way that the data is quickly written into the cell, minimizing the time during which the access transistors are on and susceptible to leakage. The additional transistors P3 and N6 assist in the write process.

P3 helps to quickly select the appropriate storage node to the desired value, while N6 ensures that the opposite storage node is effectively grounded, thereby enhancing the speed and stability of the write operation.

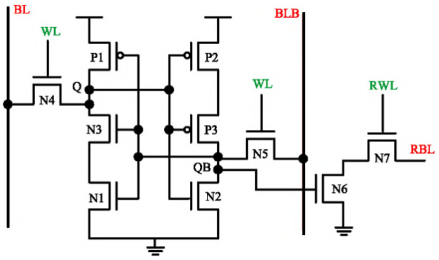

Fig. 3 – Proposed hybrid PNN-PPN 10T SRAM with LCT.

For a read operation, the RWL is activated, turning on the read access transistor N7. The storage node's value is sensed on the RBL. When RWL is high, N7 is on, and the data from the storage node (QB) is transferred to RBL. During this period, N5 remains off, ensuring that the primary storage nodes (Q and QB) are still isolated from the BL and BLB, minimizing leakage paths through the access transistors (N3 and N4). The design ensures that the read operation does not disturb the storage nodes significantly, preventing unnecessary leakage currents that might occur due to fluctuations in the storage node voltages during read access. By carefully controlling the read operation and ensuring minimal disturbance to the storage nodes, the circuit efficiently decreases leakage current during read cycles.

The hold operation is when the SRAM cell is in an idle state, retaining the stored data without any read or write activity. During the hold operation, the WL is not activated (WL is low), which means the access transistors N3 and N4 are off. N5 is turned off during the hold state, effectively isolating the Q and QB from the BL and BLB. This isolation prevents any leakage paths through the access transistors (N3 and N4) to the bit lines. When Q stores a logic 1, P2, P3, N1, and N3 are in the OFF state, and N2 and PI are in the ON state. By isolating the storage nodes, the leakage paths are significantly reduced as there is no direct connection for the leakage current to flow from the storage nodes to the bit lines. This isolation ensures that the SRAM cell maintains its data with minimal leakage current, preserving power and enhancing energy efficiency. The hybrid PNN-PPN 10T SRAM cell employs a strategic approach to minimize leakage currents through the combined action of additional transistors and the LCT. The overall architecture is optimized for low power consumption, making it suitable for advanced, energy-efficient memory applications.

3. RESULTS AND DISCUSSION

The efficiency of the proposed hybrid 10T SRAM cell is verified through detailed simulation results and waveform analysis. Key performance parameters such as PDP, leakage power, dynamic power, SNM, and delay are meticulously evaluated. To accurately design and assess the SRAM cells, the CADENCE Virtuoso tool is employed. This tool is highly regarded in the semiconductor industry for its precision and versatility in designing and simulating integrated circuits.

3.1. SIMULATION SETUP

For simulating the circuit behavior and extracting performance metrics, the Spectre simulator from Cadence Design System is used. Spectre is known for its accurate modeling of transistor-level characteristics, making it an ideal choice for this type of analysis. Figure 4 shows Test set up of proposed hybrid PNN-PPN 10T SRAM with LCT using Cadence-Virtuoso Tool. Figure 5 shows the design of proposed model. Figure 6 shows the output of proposed model obtained using Cadence-Virtuoso Tool. The output waveform of the LCT-based hybrid SRAM cell for Q and QB, with WL enabled and BL and BLB values of 1000110010 and 0111001101, is displayed in Fig. 7. Layout diagram of the proposed hybrid PNN-PPN 10T SRAM with LCT is shown on Fig. 8.

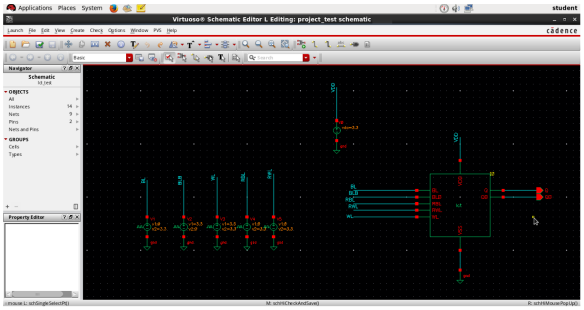

Fig. 4 – Test set up of proposed hybrid PNN-PPN 10T SRAM with LCT using Cadence-Virtuoso Tool.

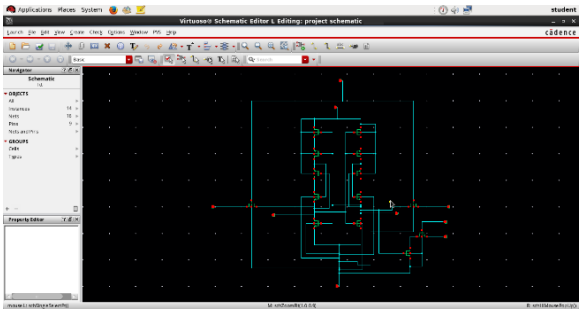

Fig. 5 – Design of proposed hybrid PNN-PPN 10T with LCT using Cadence-Virtuoso Tool.

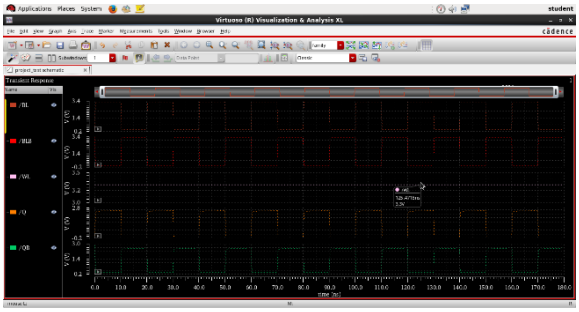

Fig. 6 – Output of Proposed SRAM with LCT using Cadence-Virtuoso Tool.

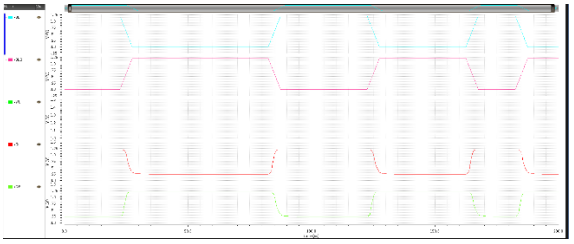

Fig. 7 – Output waveform of the proposed model.

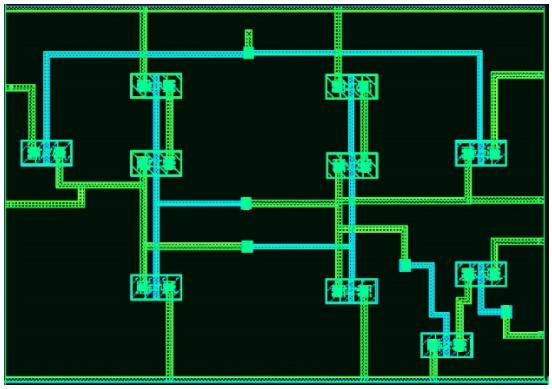

Fig. 8 – Simulation layout of hybrid PNN-PPN 10T SRAM with LCT.

3.2. PERFORMANCE METRICS

Various performance metrics are crucial for understanding the advantages and operational efficiency of the SRAM cell in multiple states: read, write, and hold operations. Table 1 provides a summary of the performance metrics employed in the proposed study.

Table 1
Performance Metrics

Parameters	Equation
$RSNM$	$\min(V_{DD}-V_{BL},V_{BL})-\frac{1}{2}(V_{THN}+V_{THP})$
$WSNM$	$\min(V_{DD}-V_{BL},V_{BL})-\frac{1}{2}(V_{THN}+V_{THP})$
$HSNM$	$\min(V_{DD}-V_{BLH},V_{BLH})-\frac{1}{2}(V_{THNH}+V_{THPH})$
PDP	$Power \times propagation\ delay$
P_{leak}	$V_{DD}I_{leak}$
$P_{dynamics}$	$\alpha C_L V^2{}_{dd} f$

V_{BL} bitline swing $V_{BLH}$is the bitline swing in hold operation, , and $V_{THPH}$is the threshold voltage for the transistors in the hold path in NMOS and PMOS, respectively.

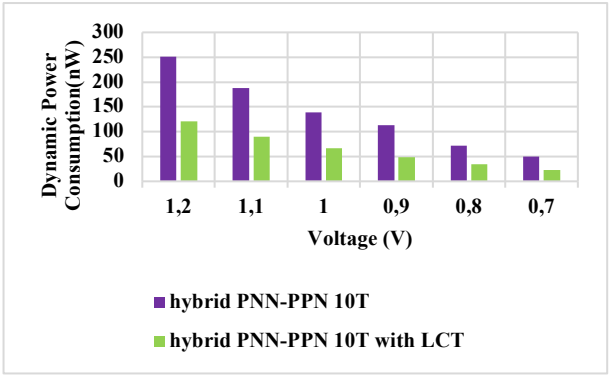

Fig. 9 – Dynamic power consumption.

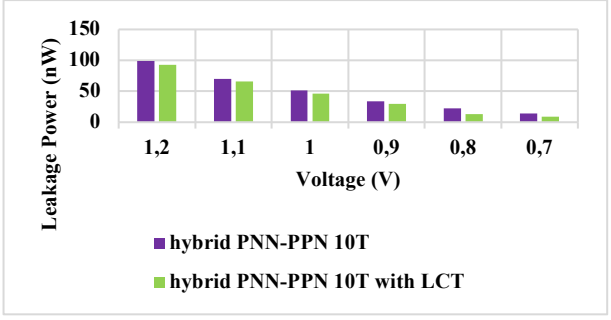

Fig. 10 – Leakage Power.

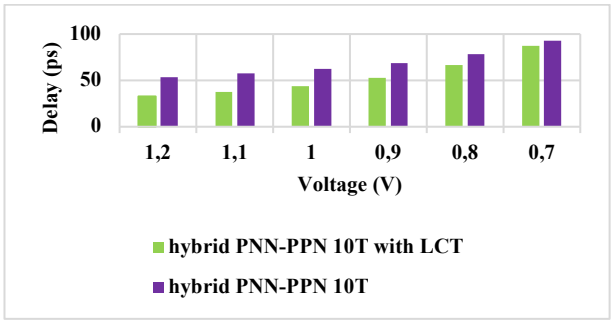

Fig. 11 – Delay.

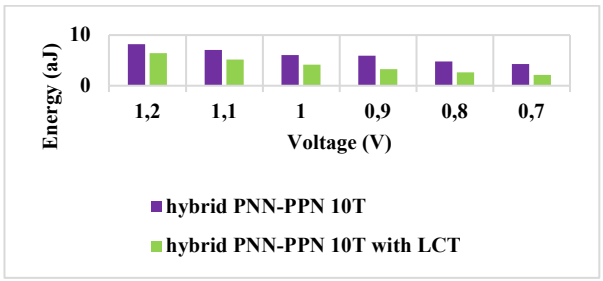

Fig. 12 – Power Delay product.

Figure 9 shows the plot of dynamic power consumed for different voltages. Figure 10 shows the plot of leakage power for other voltages. Figure 11 shows the plot of delay for different voltages. The plot of the power delay product at various voltages is displayed in Fig. 12.

The hybrid PNN-PPN 10T SRAM with LCTs is shown in Fig. 13 with its RSNM measured at 319.315 mV. The hybrid PNN-PPN 10T SRAM with LCTs is demonstrated in Fig. 14's WSNM butterfly curve, with the WSNM measured at 43.3495 mV. The hybrid PNN-PPN 10T SRAM with LCTs is shown in Fig. 15's HSNM butterfly curve, with the HSNM measured at 291.137 mV.

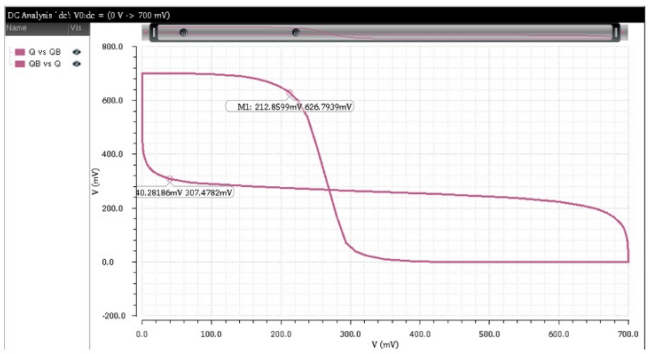

Fig. 13 – RSNM for the proposed method.

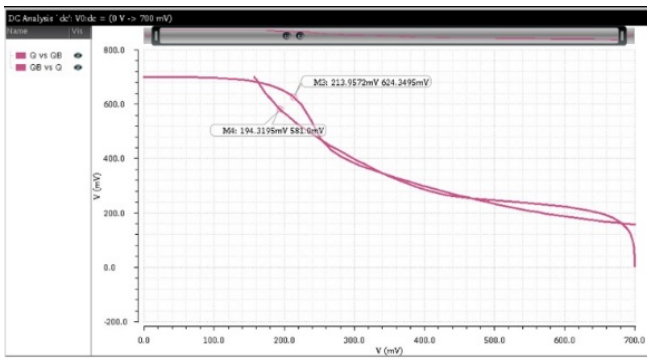

Fig. 14 – WSNM for the proposed method.

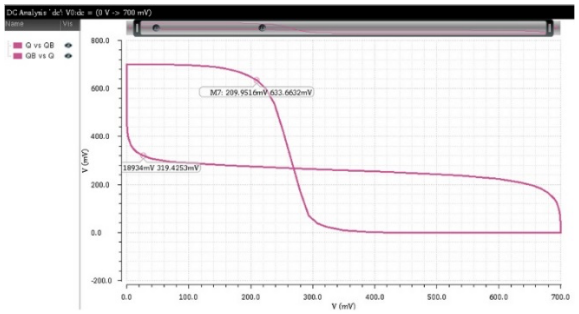

Fig. 15 – HSNM for the proposed method.

4. CONCLUSION

The proposed study introduces a novel hybrid PNN-PPN 10T SRAM architecture augmented with Leakage Control Transistors (LCTs) to tackle the critical issue of leakage in semiconductor memory designs. Leakage power, a key concern during standby modes, is effectively mitigated through strategic transistor configurations and the integration of LCT. Challenges in existing methods include inadequate leakage current control and compromised energy efficiency, particularly in low-power tasks. The study employs meticulous simulation using Cadence Virtuoso to evaluate delay, dynamic power, leakage power, and PDP. Results demonstrate the superiority of the hybrid architecture with LCTs, exhibiting reduced dynamic and leakage power, lower delay, and an enhanced power-delay product compared to conventional approaches. SNM evaluation further validates the robustness of the proposed design against noise, ensuring reliable data retention.

Overall, the research underscores the significance of effective leakage current management for advancing energy-efficient semiconductor memory architectures, offering promising solutions to address contemporary challenges in VLSI design. Future research could explore the integration of emerging semiconductor materials, such as graphene or transition metal dichalcogenides, to further reduce leakage currents while maintaining or improving performance.

Additionally, the development of adaptive leakage control techniques that dynamically adjust to varying operational conditions could lead to even more efficient SRAM designs. Research into advanced fabrication technologies, such as FinFET and nanoscale CMOS, could offer insights into how these structures can complement the proposed hybrid SRAM design. Moreover, the applicability of this design in larger-scale systems, such as multicore processors and IoT devices, presents an exciting avenue for future work, particularly in optimizing memory for high-density and high-performance applications. Investigating the trade-offs between performance, power consumption, and reliability in such applications will be crucial to meet the ever-growing demands of modern electronic systems.

CREDIT AUTHORSHIP CONTRIBUTION STATEMENT

Anitha Bose: Conceived of the presented idea. Developed the theory and performed the computations.

Santhi Nagarajan: Verified the analytical methods. Produced the results and contributed to the final manuscript.

Received on 22 August 2024

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