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A GENERALIZED MULTISOURCE SYMMETRICAL MULTILEVEL INVERTER WITH REDUCED SWITCHES

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Keywords: Multilevel inverters; Multisource; Phase disposition; Level shifted; Pulse width modulation; Symmetrical; Total harmonic distortion.

This paper proposes a generalized multisource symmetrical multilevel inverter with reduced switches. The proposed topology uses fewer switches, thereby minimizing switching losses and improving system efficiency. The salient features of this topology are the elimination of diodes and capacitors, a reduced number of switches, the ability to expand the circuit to achieve as many levels as needed, reduced total standing voltage (TSV), reduced cost, and lower Total Harmonic Distortion (THD). The phase-disposition level-shifted pulse-width modulation technique is used, and logic gates are employed to generate triggering pulses. The proposed topology is simulated in MATLAB/Simulink for 11 levels, with 5 DC sources and nine switches. The performance analysis for the resistive and inductive loads was performed. I have also provided a detailed comparison with other recent research works to demonstrate the effectiveness of the proposed system. The proposed topology is also realized using the hardware for an 11-level output.

1. INTRODUCTION

The multilevel inverters offer a compelling option for high-power, medium-voltage applications by integrating multiple small voltage levels to produce a stepwise voltage output [1]. The multilevel inverters provide common-mode voltage, reducing the motor's stress without damaging it. Multilevel inverters have become popular due to their ability to operate at both fundamental and high switching frequencies, as well as their reduced electromagnetic interference and lower input current distortion. Multilevel inverters are used in electric motors, electric cars, flexible AC transmission systems (FACTS), solar photovoltaic systems, aeroplanes, and many more. In 1975, the first multilevel inverter with a three-level output was released. Clamping diodes were employed in neutral-point or diode-clamped multilevel inverter circuits; however, their intricate design and high reverse-recovery stress were drawbacks. By substituting capacitors for the diodes, the problems above were resolved. This design is known as a flying capacitor topology. However, the exorbitant cost of capacitors and problems with capacitor voltage balancing prevented this design from being used. A cascaded H-bridge multilevel inverter design is offered as a solution that addresses the drawbacks of the other two topologies. However, each H-bridge requires a single DC supply, and the circuit is more expensive due to the complexity of the control circuitry. Numerous innovative topologies, including modular topologies [2], fault-tolerant topologies [2], switched-capacitor topologies, symmetrical and asymmetrical topologies [19], reduced-switch-count topologies, etc., have emerged from ongoing studies of multilevel inverters. [3–6] covers multilevel inverters with switched-capacitor topologies. Some benefits of switched-capacitor multilevel inverters include the ability to increase voltage gain, operate at higher switching frequencies, provide accurate load control, eliminate the need for massive inductors, and utilise a single DC source. However, employing a switched-capacitor-based inverter presented several issues, including capacitor voltage balancing, the potential for voltage ripples during charging, and a complex control circuit. As a result, careful capacitor design is required to lower the voltage ripple.

In [7], a hybrid structure was developed, connecting a two-level inverter through a transformer to a cascaded H-bridge inverter. By appropriately choosing the transformer turns ratio, the inverter may be operated in either symmetric or asymmetric mode. However, due to transformer saturation, this topology is limited to constant-frequency applications and cannot be employed over a wide frequency range. In [8], a unique three and 5-level T-type inverter design was presented. The paper assumes perfectly balanced capacitor voltages, which may not hold in real-world situations.

Additionally, the effects of unbalanced voltages on the effectiveness of T-type inverters were not considered, even though the topology requires fewer power devices than other topologies of the same power level and is highly efficient in grid-connected applications. Because it has fewer switches and voltage sources than traditional topologies, the innovative generalised topology presented in [9] is considered very efficient. However, the influence of topology on system cost was not considered, and the research did not give experimental confirmation of the simulation results. The modular multilevel structure for solar photovoltaic applications covered in [10] can produce a distortion-free sinusoidal output voltage with lower losses. However, the suggested topology's limitations regarding scalability and adaptation to varying power levels and grid situations are not covered. In addition to these topologies, other circuits that use distinct level- and polarity-generating circuits include multilevel DC links, crisscross, and series-linked switching sources. Other multilevel inverter arrangements that developed as a result of intensive study included hexagon switch cell structures, ladder-based structures, stacked configurations with and without level-doubling networks, unit-based reduced-switch-count multilevel inverters, and compact module configurations. The novel generalised symmetrical multisource topology proposed in this research has the following benefits:

- Fewer switches in comparison to other topologies.
- Simply expanded to create additional levels without requiring significant structural changes.
- Separate polarity and level generation circuits are not required.
- To create any necessary level, just three switches are to be in an active state.
- It decreases the total standing voltage.
- In comparison to other typical topologies, there is also a reduction in the overall harmonic distortion.

The structure of this document is as follows: The suggested topology and the switching states are described in Section 2. The phase disposition modulation approach was described in Section 3. Section 4 discussed the logic gate implementation, while Section 5 describes the extension of the suggested

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topology. Section 6 covers the findings and their implications. Section 7 addresses the paper's conclusion.

2. PROPOSED TOPOLOGY

Figure 1 below depicts the innovative architecture for the 11-level multilevel inverter.

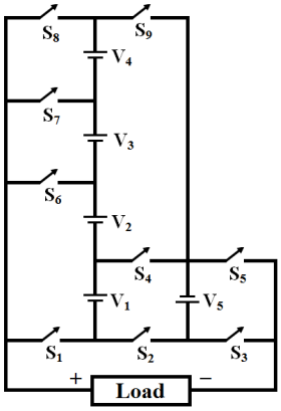


Fig. 1 – Proposed topology for 11 levels.

Eleven levels have been generated by the circuit using nine switches (S_1 to S_9) and five voltage sources (V_1 to V_5) of equal magnitude V_{dc}. Three of the nine switches (S_4, S_5, S_6) are bidirectional, and the remaining six are unidirectional. A good selection of the switching sequence might produce the requisite voltage levels. Because there are equal voltage sources across the circuit, it is called a symmetrical multilevel inverter topology. Table 1 below illustrates the proposed multilevel inverter's switching states. It should be mentioned that in order to produce any necessary level, only three switches will be active all at once.

Table 1

Switching states.

Figure	Output voltage	Active switches
a	V_{dc}	S_4, S_5, S_6
b	$2V_{dc}$	S_4, S_5, S_7
c	$3V_{dc}$	S_2. S_5, S_6
d	$4V_{dc}$	S_2, S_5, S_7
e	$5V_{dc}$	S_2. S_5, S_8
f	$-V_{dc}$	S_1, S_4, S_5
g	$-2V_{dc}$	S_1.S_3, S_4
h	$-3V_{dc}$	S_3, S_6, S_9
i	$-4V_{dc}$	S_1, S_5, S_9
j	$-5V_{dc}$	S_1, S_3, S_9

Figure 2 depicts the actual current direction for each of the levels. The switches S_2, S_5, and S_8 are activated to provide a +5 Vdc voltage. Current flows from V_1-V_2-V_3-V_4-S_8-Load-S_5-V_5-S_2-V_1, the five voltage sources being linked in series. In the same way, the current flows from V_1-V_2-V_3-V_4-S_9-V_5-S_3-Load-S_1-V_1, and the switches S_1, S_3, and S_9 are activated. All voltage sources are linked in series in this mode as well, but the polarity reverses when the current direction reverses. Similarly, as seen in Table 1, various switching patterns can produce various voltage values. The circuit operation of all the levels is shown in fig. 2 below. It is evident from the circuits above that the topology is made so that, with the right choice of switches to be turned ON and OFF, the output voltage's polarity may be changed, eliminating the need for a separate polarity generator module altogether. Because of this, both the price and the size are decreased.

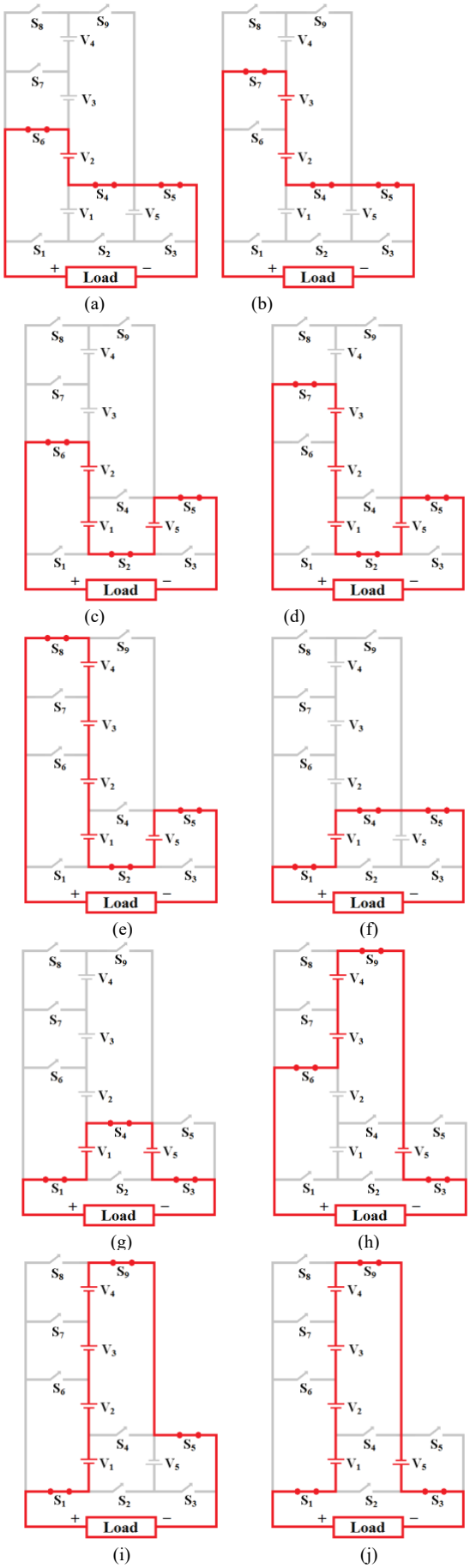


Fig. 2 – Current flow path for the voltage level of: (a)V_{dc}; (b) $2V_{dc}$; (c)$3V_{dc}$; (d) $4V_{dc}$; (e) $5V_{dc}$; (f)-V_{dc}; (g) – $2V_{dc}$; (h) -$3V_{dc}$; (i) -$4V_{dc}$, and (j) -$5V_{dc}$.

3. PHASE DISPOSITION LEVEL SHIFTED PULSEWIDTH MODULATION

Pulse width modulation (PWM) is the process of varying the width of the gate pulses to regulate the average output voltage. Either the fundamental switching frequency or a high switching frequency can be used for modulation. Space vector PWM (SVPWM), selective harmonics elimination PWM (SHEPWM), and multicarrier PWM are further classifications of high-switching-frequency modulation. This research uses multicarrier PWM.

This suggested design uses level-shifted PWM under the multicarrier technique. Techniques for level-shifted pulse-width modulation fall into three categories. Phase disposition (PD), phase opposition disposition (POD), and alternative phase opposition disposition (APOD) are their types. In this circuit, all three techniques were employed and compared. It is found that phase-disposition level-shifted pulse-width modulation provides better power quality by reducing total harmonic distortion.

The necessary number of carriers is equal to (n-1) where n is the number of levels. The device's switching period has an inverse relationship with the carrier wave frequency. The carriers are selected as triangle waves with the same peak-to-peak amplitude and phase, spanning the full voltage range. The first carrier covers the range from 0 to V_{dc}, the second from V_{dc} to $2V_{dc}$, and so on.

These carriers are placed vertically. Likewise, the negative cycle of the output voltage is covered by the waves below the zero axis. The magnitude of the carrier waves remains constant, whereas their phases change in the POD and APOD techniques. Ten carrier waves were selected for this study, five of which were employed for the positive cycle and five for the negative cycle, as seen in Fig. 3. The carrier waves for the positive half cycle are denoted by P_1 through P_5, and for the negative half cycle, by N_1 through N_5. The frequency of the sine wave (f_m) is 50 Hz, and the frequency of the carrier wave (f_c) is 1 kHz. The amplitude of the sine wave (A_s) is 5 V, and the amplitude of the carrier wave is taken as 1 V each. Gating pulses are produced through the comparison of the carrier signal with the sinusoidal signal. The switches receive these gating pulses according to the switching sequence, producing the necessary output levels.

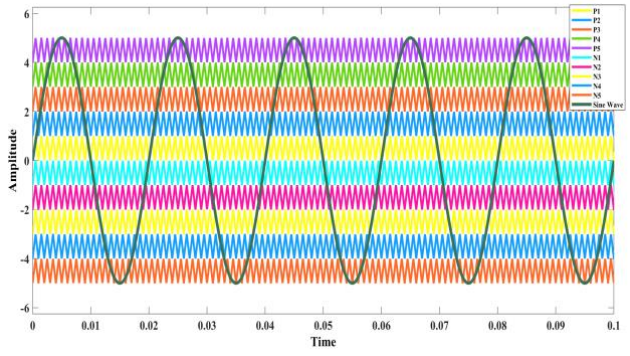


Fig. 3 – Phase disposition level shifted pulse width modulation.

4. LOGIC GATES IMPLEMENTATION

In this topology, the number of gating pulses generated equals the number of carrier signals, or 10. Nine switches, however, are fewer than the total number of pulses generated. Operating the switches with the available output pulses thus becomes hard. Thus, the gating pulse circuit is implemented using simple logic gates. Equations 1 through 9 represent the logical expressions to generate pulses to the respective switches. The logical expressions are obtained from the switching pattern for the proposed topology.

$$S_1 = \overline{N_1 \oplus N_2 \oplus N_3}, \quad (1)$$

$$S_2 = P_3, \quad (2)$$

$$S_3 = \overline{N_2 \oplus N_4 \oplus N_5}, \quad (3)$$

$$S_4 = (P_1 \oplus P_3) + (N_1 \oplus N_3), \quad (4)$$

$$S_5 = P_1 + (N_1 \oplus N_2) + (N_4 \oplus N_5), \quad (5)$$

$$S_6 = (P_1 \oplus P_2) + (P_3 \oplus P_4) + (N_3 \oplus N_4), \quad (6)$$

$$S_7 = (P_2 \oplus P_3) + (P_4 \oplus P_5), \quad (7)$$

$$S_8 = P_5, \quad (8)$$

$$S_9 = \overline{N_3}, \quad (9)$$

where P_1 to P_5 represent the carrier waves for positive half cycles and N_1 to N_5 represent the carrier waves for negative half cycles.

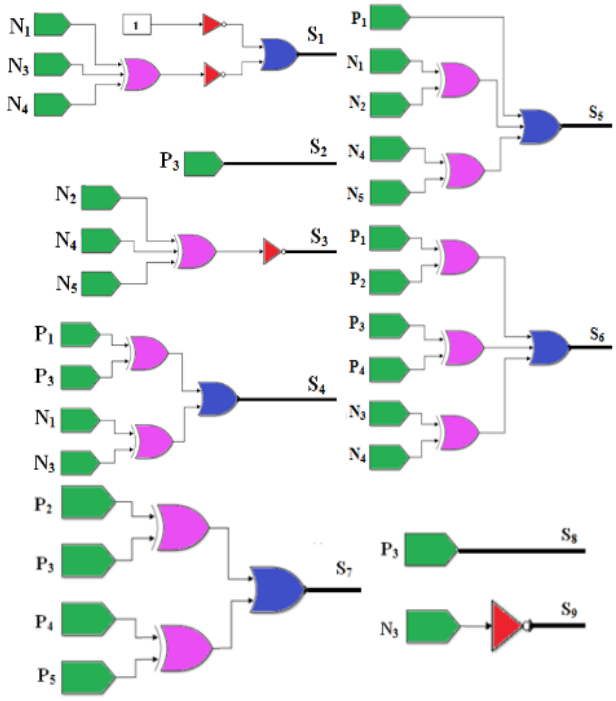


Fig. 4 – Implementation of pulse generation circuit using logic gates from S_1 to S_9, respectively.

Once the logical statements for each switch are derived, the corresponding gates can be used to build the gate driver circuit. Fig. 4 illustrates how the logic gates are used to implement logical functions.

5. EXTENSION OF PROPOSED TOPOLOGY

The fact that the suggested design may be expanded to include more levels by including switches and voltage sources is one of the advantages it offers. Fig. 5 below shows the expanded circuit diagram required to achieve the desired number of levels. The switches are represented by S_1, S_2… S_{k-2}, S_{k-1}, and S_k, and the voltage sources are represented by V_1, V_2…V_{n-1}, V_n.

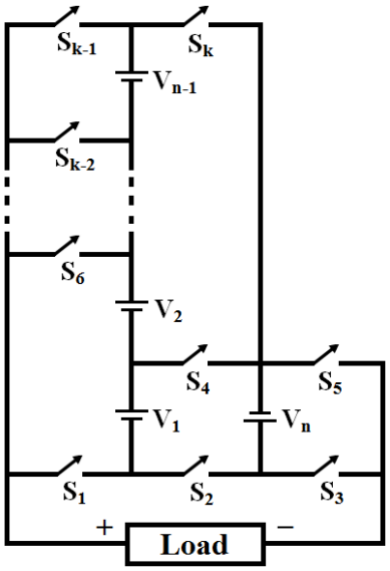


Fig. 5 – Extension of proposed topology.

Let 'n' be the number of sources, 'm' be the number of levels, and 'k' be the number of switches; then the number of sources(n) required to generate 'm' levels is given by:

$$n = \frac{m-1}{2} \quad (10)$$

The number of switches (k) and the number of levels (m) are related by:

$$k = \frac{m+7}{2} \quad (11)$$

The above equations can also be rewritten in terms of the number of sources. If there are 'n' number of sources, then the number of levels is given by:

$$m = 2n + 1. \quad (12)$$

The number of switches (k) needed for a circuit with 'n' sources is given by:

$$k = n + 4. \quad (13)$$

To raise the number of levels by two in this architecture, one switch and one DC source must be added. It is therefore possible to determine the required number of switches and DC sources by setting the number of levels. Likewise, the number of levels and switches may be determined by setting the number of DC sources.

6. COMPARISON OF PROPOSED TOPOLOGY WITH CONVENTIONAL TOPOLOGIES

The proposed topology is compared with other topologies in the literature and summarized in Table 2. For the same levels, it was understood that the proposed topology has fewer switches. The number of sources may be higher than in other topologies. Still, eliminating capacitors in the proposed topology avoids the problems of capacitor voltage balancing and inrush currents.

The total standing voltage is the sum of all the blocking voltage capabilities for all switches in a certain topology:

$$TSV = \sum_{i=1}^{n} V_k, \quad (14)$$

where 'n' is the number of switching devices and V_k is the blocking voltage of different switches.

Table 2

Comparison with other topologies.

Paper / Parameters	n	k	N_C	N_{di}	TSV
[3]	1	m+1	$\frac{m-1}{2}$	$\frac{m-1}{2}$	NA
[11]	1	2(m+1)	m-1	m-1	7m-4
[12]	$\frac{3(m-1)}{2}$	$\frac{8(m-1)}{5}$	0	0	$\frac{12(m-1)}{5}$
[13]	$\frac{m-1}{5}$	m-1	$\frac{2(m-1)}{5}$	0	$\frac{9(m-1)}{5}$
[14]	1	$\frac{3m-1}{2}+5$	m-2	m-2	NA
[15]	$\frac{m-1}{4}$	$\frac{3m+5}{4}$	$\frac{m-1}{2}$	$\frac{m-1}{4}$	2(m-1)
[16]	1	$\frac{3m+1}{2}$	$\frac{m-1}{2}$	0	3(m-1)
[17]	1	2(m-1)	$\frac{1(m-3)}{2}$	0	NA
Proposed	$\mathbf{\frac{m-1}{2}}$	$\mathbf{\frac{7+m}{2}}$	**0**	**0**	$\mathbf{7(\frac{m-1}{3})}$

m-number of levels ; n- number of DC sources; k-number of switches; N_C-Number of capacitors; N_{di}- Number of diodes; TSV – Total Standing voltage; NA-Not Addressed

The maximum blocking voltage of switches is as follows:

$$S_3=S_5=S_7= V_{dc}, \quad (15)$$

$$S_4 = S_6= S_8 = 2V_{dc}, \quad (16)$$

$$S_1 = 4V_{dc}, \quad (17)$$

$$S_2 = S_9 = 5V_{dc}. \quad (18)$$

Hence, the TSV of the proposed topology that generates an 11-level output is given by:

$$TSV = \sum_{i=1}^{9} V_k =$$

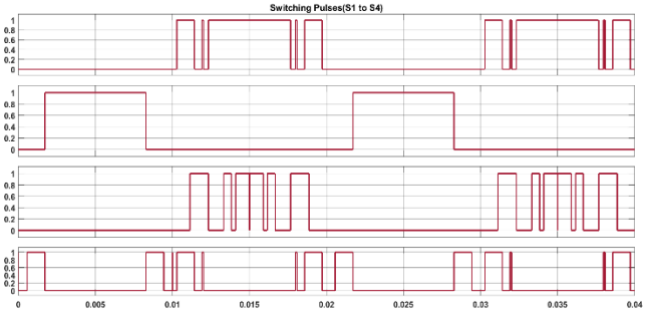
$$= 3V_{dc} + (3 \times 2V_{dc}) + 4V_{dc} + (2 \times 5V_{dc}) =$$

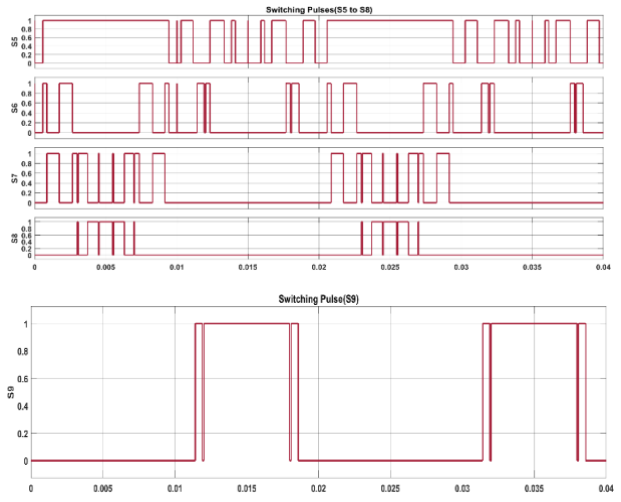
$$= 23V_{dc} \quad (19)$$

The total standing voltage is less than [11] but slightly higher than [13]. Still, the use of more capacitors in [13] makes it less reliable than the proposed topology.

7. RESULTS & DISCUSSION

The proposed topology was simulated using MATLAB/Simulink software. The value of the voltage sources is considered as 100 V each for simulation purposes. The gating pulses for the nine switches are generated using a level-shifted pulse-width modulation technique. The output voltage, output current, and the fast Fourier transform (FFT) analysis for a pure resistive load of 10KΩ are shown in Fig. 6.





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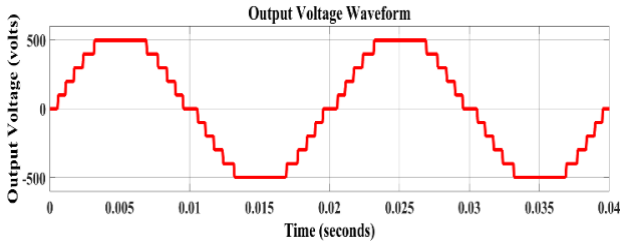

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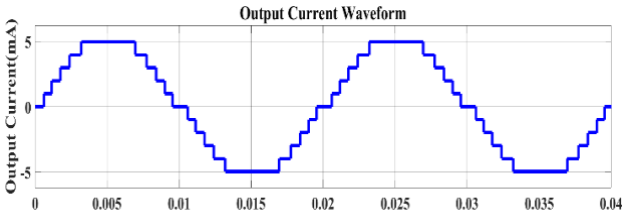

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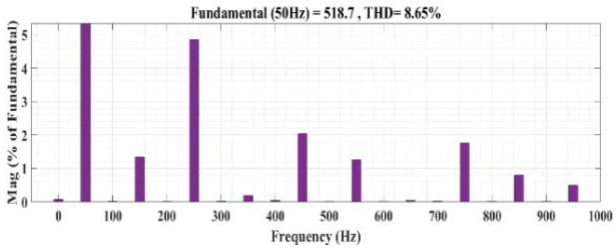


(d)

Fig 6 – Simulation results of an 11-level inverter; a) Switching pulses; b) Output voltage waveform for R = 10 kΩ; c) Output current waveform for R =100 kΩ, and d) FFT analysis of the output voltage of the 11-level inverter for R = 100 kΩ.

The output voltage is smoother at higher levels than with a conventional 2-level inverter.

The total harmonic distortion for the 11-level inverter is calculated using the FFT analyzer. The total harmonic distortion was found to be 8.66%. The comparison between phase disposition (PD), phase opposition disposition (POD), and alternative phase opposition disposition (APOD) pulse width modulation techniques for the pure resistive (R) and resistive-inductive (RL) load was represented in Table 3. A resistance of 10 kΩ and an inductor of 15mH are considered for the load values for simulation. It is observed that the phase disposition technique reduces the harmonics compared to other techniques.

Table 3

Comparison of THD with PD, POD, and APOD PWM techniques

Modulation Technique	THD (%)	
	R	RL
PD	8.66	8.65
POD	10.76	10.77
APOD	10.07	10.40

The simulated results are verified using the laboratory prototype model shown in Fig. 7 using a resistive load of 10 kΩ.

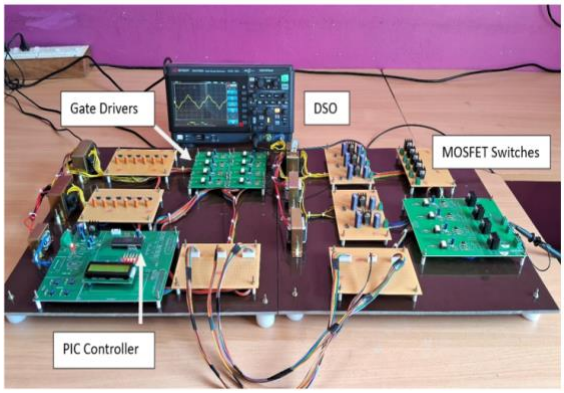


Fig. 7 – Laboratory prototype of an 11-level inverter.

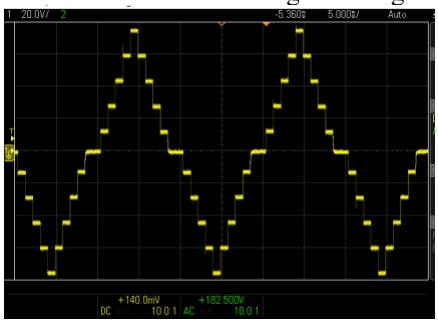
The hardware details are mentioned in Table 4.

Table 4

Hardware details.

Component	Part Number
Microcontroller	DSPIC30F4011
MOSFET Switches	IRF840
MOSFET Driver Circuit	TLP250
Resistive Load	10 kΩ

There are 9 MOSFETS used and 9 gate driver circuits. The five symmetrical DC sources are obtained from transformers and then rectified using the bridge rectifier.



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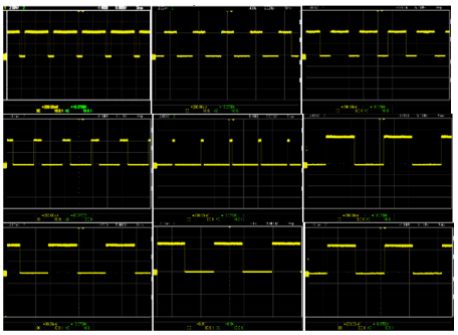

(b)

Fig.8 – Experimental results; a) 11-level output voltage waveform, b) Switching pulses to the switches S_1 to S_9.

The rectified output is filtered and given to the gate driver circuits. The experimental results are found to be similar to the simulation results. The gate signals and the output voltage waveform obtained using the laboratory prototype are shown in Fig. 8.

8. **CONCLUSION**

The proposed symmetrical multilevel inverter that generates an 11-level output voltage uses fewer switches and reduces total harmonic distortion to 8.65%. Capacitors and diodes are eliminated in this topology, resulting in reduced switching losses and increased efficiency. The proposed circuit can be extended to increase the number of levels effectively without major changes to the overall structure. Comparing the proposed generalized circuit with other similar proposals showed that the proposed topology is better, with fewer switches and a lower total standing voltage. The simulated results are validated using the laboratory prototype. Because the topology uses multiple voltage sources, it is well-suited to solar photovoltaic and hybrid renewable energy applications. Asymmetrical circuit operation can be achieved by connecting two modules in series, which is considered a future scope of work.

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